6427 101922

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 8/20/03 Serial # 10/013,103 Priority Application Date 6/26/98

Your Name M. Lewis Examiner # _____

AU 2829 Phone 305-3743 Room Plaza 3-3805

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

08-21-03 A09:50 IN

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 17-24

Problem: see Page 2 lines 6-26
" 3 " 1-6

Solution: " " 4 " 1-6

Please look for the specific compounds utilized

Staff Use Only
Searcher: Heck Rand
Searcher Phone: _____
Searcher Location: STIC-EIC2800, CP4-9C18
Date Searcher Picked Up: 9/25/03
Date Completed: 9/25/03
Searcher Prep/Rev Time: 155
Online Time: 95

Type of Search
Structure (#)_____
Bibliographic ✓
Litigation_____
Fulltext_____
Patent Family_____
Other_____

Vendors
STN ✓
Dialog ✓
Questel/Orbit_____
Lexis-Nexis_____
WWW/Internet_____
Other _____

```
 25aug03 09:50:43 User267149 Session D940.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2003/Aug W2
         (c) 2003 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2003/Aug W4
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
*File   6: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   8:Ei Compendex(R)  1970-2003/Aug W3
         (c) 2003 Elsevier Eng.  Info. Inc.
*File   8: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File  34:SciSearch(R) Cited Ref Sci  1990-2003/Aug W3
         (c) 2003 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2003/Jul
         (c) 2003 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2003/Aug W3
         (c) 2003 BLDSC all rts. reserv.
  File  94:JICST-EPlus  1985-2003/Aug W4
         (c)2003 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2003/Jul
         (c) 2003 The HW Wilson Co.
  File 144:Pascal  1973-2003/Aug W2
         (c) 2003 INIST/CNRS
  File 305:Analytical Abstracts  1980-2003/Jul W4
         (c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2003/Jul
         (c) 2003 DECHEMA
  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200354
         (c) 2003  Thomson Derwent
  File 347:JAPIO  Oct 1976-2003/Apr(Updated 030804)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2003/Mar
         (c) 2003 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

Set	Items	Description
S1	539	AU=(SESHAN, K? OR SESHAN K?)
S2	58	AU=(DASS, M? OR DASS M?)
S3	232	AU=(BAKKER, G? OR BAKKER G?)
S4	6	S1 AND S2
S5	1	S4 AND S3
S6	5	S4 NOT S5
S7	5	RD (unique items)
S8	57	(S1 OR S2 OR S3) AND ((INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?)) OR IC OR CHIP? ?)
S9	0	S8 AND (OXYD????????(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER-???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?))
S10	11	S8 AND ((INSULAT???????? OR DIELECTR????????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE-()LAYER? ?))
S11	11	RD (unique items)
S12	46	S8 NOT S10
S13	1	S12 AND ((SILICON OR SI)(3N)DIOXIDE OR SIO2)
S14	45	S12 NOT S13
S15	1	S14 AND ((SILICON OR SI)(3N)OXYNITRIDE OR SION)
S16	44	S14 NOT S15
S17	0	S16 AND ((SILICON OR SI)(3N)NITRIDE OR SI3N4)

5/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014725215
WPI Acc No: 2002-545919/200258
XRAM Acc No: C02-154711
XRPX Acc No: N02-432061
Passivation of integrated circuit devices for wire bond packaging, involves forming adhesion layer on surface of insulating layer by treating surface of insulating layer with gas
Patent Assignee: INTEL CORP (ITLC)
Inventor: **BAKKER G L; DASS M L A; SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6352940	B1	20020305	US 98105590	A	19980626	200258	B

Priority Applications (No Type Date): US 98105590 A 19980626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6352940	B1		17	H01L-021/31	

Abstract (Basic): US 6352940 B1
Abstract (Basic):
NOVELTY - An integrated circuit (IC) device is passivated by forming an insulating layer (28) on a substrate (26). An adhesion layer (150) is formed into the surface of the insulating layer by treating the surface of the insulating layer with a gas. A first passivation layer is formed on the adhesion layer. The first passivation layer and the gas include common chemical element(s).
USE - For passivation of IC devices used in wire bond packaging.
ADVANTAGE - The inventive method improves adhesion between insulating layer and hard passivation layers of integrated circuit devices to reduce delamination that occurs during the manufacturing process of these devices, such as thermal cycling and sawing.
DESCRIPTION OF DRAWING(S) - The figures show the inventive integrated circuit devices.
Substrate (26)
Insulating layer (28)
Adhesion layer (150)
pp; 17 DwgNo 9, 10/21

FWI

7/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015309631
WPI Acc No: 2003-370565/200335
Related WPI Acc No: 2001-069759
XRPX Acc No: N03-295530
Probe card for integrated circuit bond pad testing, has probing beams with first ends coupled to PCB and second ends extending from the sloped sidewall of the probe assembly
Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; KARKLIN K D; ROGGEL A; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6515358	B1	20030204	US 97941795	A	19970930	200335	B
			US 2000651388	A	20000829		

Priority Applications (No Type Date): US 97941795 A 19970930; US 2000651388 A 20000829
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6515358	B1		25	H01L-023/06	Div ex application US 97941795 Div ex patent US 6143668

Abstract (Basic): US 6515358 B1
Abstract (Basic):
NOVELTY - Probing beams (230) have their first ends coupled to the printed circuit board (210) and their second ends extending from the sloped sidewall of the probe assembly (220). The beams are divided into two sets, with each set of beams extending from the sidewall portion at corresponding angles relative to the horizontal plane.
USE - For testing bond pad of integrated circuit.
ADVANTAGE - Reduces or eliminates the need for periodic tweaking or positional adjustment of the probe feature position during the life of the probe card due to uniform mechanical stresses between probe layers, thus facilitating greater availability for testing procedures. Provides more consistent outtravel. Allows better scrubbing and better contact with the bond pad due to tighter distribution of tip lengths. Reduces mutual inductance in the probe assembly between the power/signal probes and their complementing ground probe. Maintains and repeats nominal probe to bond pad contact resistance below standard level to allow consistent, repeatable testing of integrated circuit devices, thus allowing a higher degree of re-sort repeatability.
DESCRIPTION OF DRAWING(S) - The figure shows the schematic planar cross-sectional view of the probe card.
Printed circuit board (210)
Probe assembly (220)
Probing beams (230)
pp; 25 DwgNo 20/24

7/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014676912
WPI Acc No: 2002-497969/200253
XRAM Acc No: C02-141137
XRPX Acc No: N02-394050
Wafer cutting apparatus for semiconductor chip manufacture detects variations in height of wafer to control motor and to vary the sawing of wafer in selected direction
Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; GAETA I S; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6357330	B1	20020319	US 99227493	A	19990107	200253	B

Priority Applications (No Type Date): US 99227493 A 19990107
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6357330	B1		14	B23D-005/30	

Abstract (Basic): US 6357330 B1
Abstract (Basic):
NOVELTY - A detector (116) facing a surface of a wafer (114) provided on a wafer holder (136) detects the variations in height of the wafer along a selected direction. Based on the variations, a central control unit (118) controls motors (154,156) independently to vary the rotational speed of corresponding sawing blades (158,160) mounted on a spindle (157) to saw the wafer in the selected direction.
USE - For semiconductor chip manufacture.
ADVANTAGE - Wafer is effectively sawed based on the variations of the height of the wafer.
DESCRIPTION OF DRAWING(S) - The figure shows the wafer cutting apparatus.
Wafer (114)
Detector (116)
Central control unit (118)
Wafer holder (136)
Motors (154,156)
Spindle (157)
Sawing blades (158,160)
pp; 14 DwgNo 3/9

7/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013595490
WPI Acc No: 2001-079697/200109
XRAM Acc No: C01-022842
XRPX Acc No: N01-060655
Test of an integrated circuit device for their functionality involves depositing a solder bump on a surface of a bond pad on an integrated circuit device, heat treating the solder bump, and testing the integrated circuit device
Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; ROGGEL A; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6162652	A	20001219	US 971969	A	19971231	200109	B

Priority Applications (No Type Date): US 971969 A 19971231
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6162652	A		13	H01L-021/66	

Abstract (Basic): US 6162652 A
Abstract (Basic):

NOVELTY - An integrated circuit device is tested by depositing a solder bump (150) on a surface of a bond pad on an integrated circuit device, heat treating the solder bump to transform the surface of the bump from rough to smooth, and testing the integrated circuit device by probing the solder bump.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of preparing a solder bump for testing.

USE - For testing an integrated circuit device to evaluate their functionality.

ADVANTAGE - Allows designers to evaluate the functionality of new devices during development, testing reliability and functionality of each die on a wafer before incurring the higher costs of packaging, performance of the production process to be evaluated, and production consistency to be rated.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic illustration of the integrated circuit device showing the processing step of electrically testing the solder bump.

solder bump (150)

pp; 13 DwgNo 16/18

7/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013585552
WPI Acc No: 2001-069759/200108
Related WPI Acc No: 2003-370565
XRAM Acc No: C01-019292
XRPX Acc No: N01-052717

Method for exposing bond pad in integrated circuit having two passivation layers, involves removing portion of second passivation layer over bond pad, curing remaining second passivation layer and etching exposed first passivation layer

Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; KARKLIN K D; ROGGEL A; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6143668	A	20001107	US 97941795	A	19970930	200108	B

Priority Applications (No Type Date): US 97941795 A 19970930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6143668	A		25	H01L-021/31	

Abstract (Basic): US 6143668 A
Abstract (Basic):

NOVELTY - A bond pad (110) in an integrated circuit coated with

first (120) and second (130) passivation layers is exposed by removing a portion of the second passivation layer over the bond pad, curing the remaining portions of the second passivation layer and etching the exposed first passivation layer to expose the bond pad.

USE - The method is used in fabrication of integrated circuit devices such as a probe card having a pad pitch of less than 80 micron.

ADVANTAGE - The method produces durable probe features with reliable contacts to bond pads having a low pad pitch.

DESCRIPTION OF DRAWING(S) - The drawing shows a stage for removal of the first passivation layer.

Aluminum bond pad (110)
Hard passivation layer (120)
Photodefinable polyimide passivation layer (130)
Residual layer following the polyimide curing step (140)
pp; 25 DwgNo 14/24

7/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013144897
WPI Acc No: 2000-316769/200027
XRAM Acc No: C00-095704
XRPX Acc No: N00-237763
Passivating integrated circuit comprises depositing silicon nitride over a top surface portion of the circuit, and treating the exposed surface to form silicon oxynitride
Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; GAETA I; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6046101	A	20000404	US 971970	A	19971231	200027	B

Priority Applications (No Type Date): US 971970 A 19971231
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6046101	A		13	H01L-021/318	

Abstract (Basic): US 6046101 A
Abstract (Basic):

NOVELTY - Integrated circuit is passivated by depositing a silicon nitride layer over the top surface of a portion of an integrated circuit, treating an exposed surface of the first passivation layer to form a silicon oxynitride layer and depositing a second passivation layer over the first passivation layer.

USE - For passivating integrated circuit.

ADVANTAGE - Delamination is minimized by eliminating passivation material from the scribe street area prior to separating devices and the combined passivation technology has robust passivation resistance to thin film delamination.

pp; 13 DwgNo 0/21

11/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03897395 INSPEC Abstract Number: B91038124
Title: Engineering change (EC) technology for thin film metallurgy on polyimide films
Author(s): Ray, S.K.; **Seshan, K.**; Interrante, M.
Author Affiliation: IBM, East Fishkill, NY, USA
Conference Title: 1990 Proceedings. 40th Electronic Components and Technology Conference (Cat. No.90CH2893-6) p.395-400 vol.1
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA 2 vol. xvi+1125 pp.
U.S. Copyright Clearance Center Code: 0569-5503/90/0000-0395$01.00
Conference Sponsor: IEEE; Electron. Ind. Assoc
Conference Date: 20-23 May 1990 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: Engineering change in multichip modules such as the IBM Thermal Conduction Module (TCM) requires making new nets on the top surface of the module. This is done either to repair opens or shorts in the internal nets or to correct design errors. Since the trend in multichip packaging in the high end is towards thin-film wiring with polyimide as the dielectric, wire-bond and laser delete processes compatible with thin-film metallurgy on polyimide films are required to carry out engineering change. The authors describe the results of a technology-development effort to optimize these processes on a metal/polyimide thin-film structure.
Subfile: B

11/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014725215
WPI Acc No: 2002-545919/200258
XRAM Acc No: C02-154711
XRPX Acc No: N02-432061
Passivation of **integrated circuit** devices for wire bond packaging, involves forming adhesion **layer** on surface of **insulating layer** by treating surface of **insulating layer** with gas
Patent Assignee: INTEL CORP (ITLC)
Inventor: **BAKKER G L; DASS M L A; SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6352940	B1	20020305	US 98105590	A	19980626	200258	B

Priority Applications (No Type Date): US 98105590 A 19980626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6352940	B1		17	H01L-021/31	

Abstract (Basic): US 6352940 B1
Abstract (Basic):

NOVELTY - An **integrated circuit** (**IC**) device is passivated by forming an **insulating layer** (28) on a substrate (26). An adhesion layer (150) is formed into the surface of the **insulating layer** by treating the surface of the **insulating layer** with a gas. A first passivation layer is formed on the adhesion layer. The first passivation layer and the gas include common chemical element(s).

USE - For passivation of **IC** devices used in wire bond packaging.

ADVANTAGE - The inventive method improves adhesion between **insulating layer** and hard passivation layers of **integrated circuit** devices to reduce delamination that occurs during the manufacturing process of these devices, such as thermal cycling and sawing.

DESCRIPTION OF DRAWING(S) - The figures show the inventive **integrated circuit** devices.

Substrate (26)

Insulating layer (28)

Adhesion layer (150)

pp; 17 DwgNo 9, 10/21

11/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012599475
WPI Acc No: 1999-405581/199934
XRAM Acc No: C99-119865
XRPX Acc No: N99-302307
Integrated circuit with an improved guard ring structure to prevent damage
Patent Assignee: INTEL CORP (ITLC)
Inventor: MIELKE N R; **SESHAN K**
Number of Countries: 084 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9934440	A1	19990708	WO 98US25467	A	19981201	199934	B
AU 9916162	A	19990719	AU 9916162	A	19981201	199951	
US 6137155	A	20001024	US 971397	A	19971231	200055	
TW 436924	A	20010528	TW 98121632	A	19981224	200172	
US 6376899	B1	20020423	US 971397	A	19971231	200232	
			US 2000651367	A	20000829		

Priority Applications (No Type Date): US 971397 A 19971231; US 2000651367 A 20000829
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9934440	A1	E	24	H01L-023/485	

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9916162	A	H01L-023/485	Based on patent WO 9934440
US 6137155	A	H01L-023/58	
TW 436924	A	H01L-021/31	

US 6376899 B1 H01L-023/544 Cont of application US 971397
Cont of patent US 6137155

Abstract (Basic): WO 9934440 A1
Abstract (Basic):
NOVELTY - The **integrated circuit** has a planar passivating layer formed on the terminal **dielectric layer**. This avoids the possibility of damage to the nitride layer caused by reentrant angles had the terminal metal layer with a guard ring protruded outside the terminal **dielectric layer** as is current practice.
DETAILED DESCRIPTION - **Integrated circuit** comprises: (a) substrate with at least one **dielectric layer** and metal **layer** formed on it, with the dielectric **layer** including a terminal **dielectric layer**; (b) planar passivating layer formed on the terminal **dielectric layer**.
USE - **Integrated circuits**.
ADVANTAGE - The planar passivating layer eliminates the problems of instability of guard rings formed in terminal metal layers.
DESCRIPTION OF DRAWING(S) - The drawings show a top view of an **integrated circuit**.
Die active area (501)
Via (504)
Planar passivating nitride layer (506)
Terminal **dielectric layer** (508, ILD4)
Guard wall (526)
Side of die (575)
Vias (V1-4)
Metal layers (M1-4)
Interlevel dielectric (ILD3)
pp; 24 DwgNo 5/8

11/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012599474
WPI Acc No: 1999-405580/199934
XRPX Acc No: N99-302306
Integrated circuit with guard ring
Patent Assignee: INTEL CORP (ITLC)
Inventor: LII M; **SESHAN K**
Number of Countries: 084 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9934439	A1	19990708	WO 98US25500	A	19981201	199934	B
AU 9916167	A	19990719	AU 9916167	A	19981201	199951	
US 6163065	A	20001219	US 972116	A	19971231	200102	
TW 447042	A	20010721	TW 98121541	A	19981223	200219	

Priority Applications (No Type Date): US 972116 A 19971231
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9934439	A1	E	22	H01L-023/48	

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM

TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9916167	A	H01L-023/48	Based on patent WO 9934439
US 6163065	A	H01L-023/544	
TW 447042	A	H01L-021/3205	

Abstract (Basic): WO 9934439 A1
Abstract (Basic):
NOVELTY - The **IC** (400) includes at least one **dielectric layer** (403) and a metal layer (402), formed on a substrate and forming a die active area (401). A guard ring (404) encloses the die active area. The guard ring has zigzag shaped portions at its corners (451).
USE - None given.
ADVANTAGE - Reduces mechanical or chemical damage caused to **integrated circuit** by using guard ring.
DESCRIPTION OF DRAWING(S) - The drawing shows a top view of the **IC** with a guard ring.
pp; 22 DwgNo 4/5

11/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012449126
WPI Acc No: 1999-255234/199921
XRAM Acc No: C99-074783
XRPX Acc No: N99-190009
Integrated circuit structure on a silicon wafer substrate
Patent Assignee: INTEL CORP (ITLC)
Inventor: **SESHAN K**
Number of Countries: 083 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9917365	A1	19990408	WO 98US13561	A	19980629	199921	B
AU 9882753	A	19990423	AU 9882753	A	19980629	199935	
US 6043551	A	20000328	US 97940535	A	19970930	200023	
GB 2345384	A	20000705	WO 98US13561	A	19980629	200035	
			GB 20007667	A	20000329		
TW 429508	A	20010411	TW 98111410	A	19980714	200157	
GB 2345384	B	20021106	WO 98US13561	A	19980629	200281	
			GB 20007667	A	20000329		

Priority Applications (No Type Date): US 97940535 A 19970930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9917365	A1	E	35	H01L-023/52	

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9882753	A		Based on patent WO 9917365
US 6043551	A	H01L-027/095	
GB 2345384	A	H01L-023/58	Based on patent WO 9917365

TW 429508 A H01L-021/76
GB 2345384 B H01L-023/58 Based on patent WO 9917365

Abstract (Basic): WO 9917365 A1
Abstract (Basic):
NOVELTY - The **integrated circuit** has electrically isolated metal structure formed by patterning and etching the terminal metal layer used to form a die active area. The locking structures adhere to the overlying passivation and prevent its delamination.
DETAILED DESCRIPTION - **Integrated circuit** includes a silicon substrate; dielectric **layer** and terminal metal **layer** (TML), with the **dielectric** and TML **layers** forming a die active area. The TML has a number of locking structures electrically isolated from one another and outside the die active area. A passivation layer adheres to the locking structures.
INDEPENDENT CLAIMS are included for the following:
(i) a method of forming a sealed computer **chip** by:
(a) forming a number of electrical circuits on a silicon wafer by forming device and interconnect layers including TML;
(b) forming a guard ring from the TML enclosing the die active area;
(c) forming spaced apart locking structures enclosed by the guard ring but outside the die active area;
(d) depositing a passivation layer over the locking structures and guard ring;
(ii) the **integrated circuit** as above in which each metal locking structure is located near the **IC** edge connected to a voltage supply;
(iii) a method of fabricating a sealed computer **chip** by:
(a) forming a number of electrical circuits on a silicon wafer by forming device and interconnect layers including TML;
(b) forming a guard ring from the TML enclosing the die active area;
(c) forming spaced apart locking structures from the TML, each locking structure coupled to a voltage supply Vss of **integrated circuit**;
(d) depositing a passivation layer over the locking structures and guard ring;
(iv) a device as above including a number of **dielectric** and metal **layers** forming a die active area, the **dielectric** layers and metal **layers** including terminal **dielectric** (TDL) and metal (TML) layers.
USE - Fabrication of **integrated circuits**.
ADVANTAGE - The structure reduces the possibility of sawing cuts through the guard wall and prevents interlayer delamination.
DESCRIPTION OF DRAWING(S) - The drawing shows an **integrated circuit** of the invention.
Die active area (501)
Terminal metal layer (502)
Terminal **dielectric layer** (503)
Contiguous guard ring (504)
Locking structure (506)
Corners (550)
Edges (575)
Pattern recognition structures (580)
Voltage supply (Vss)
pp; 35 DwgNo 5/12

11/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012449116
WPI Acc No: 1999-255224/199921
XRAM Acc No: C99-074776
XRPX Acc No: N99-189999
Integrated circuit structure on a silicon wafer substrate
Patent Assignee: INTEL CORP (ITLC)
Inventor: MIELKE N R; **SESHAN K**
Number of Countries: 084 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9917348	A1	19990408	WO 98US14023	A	19980706	199921	B
AU 9882916	A	19990423	AU 9882916	A	19980706	199935	
US 5977639	A	19991102	US 97940304	A	19970930	199953	
GB 2345580	A	20000712	WO 98US14023	A	19980706	200035	
			GB 20007669	A	20000329		
TW 409370	A	20001021	TW 98111409	A	19980714	200121	
GB 2345580	B	20020703	WO 98US14023	A	19980706	200251	
			GB 20007669	A	20000329		

Priority Applications (No Type Date): US 97940304 A 19970930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9917348	A1	E	32	H01L-021/283	

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9882916	A		Based on patent WO 9917348
US 5977639	A	H01L-023/48	
GB 2345580	A	H01L-023/58	Based on patent WO 9917348
TW 409370	A	H01L-021/8252	
GB 2345580	B	H01L-023/58	Based on patent WO 9917348

Abstract (Basic): WO 9917348 A1
Abstract (Basic):

NOVELTY - The **integrated circuit** has electrically isolated metal staples formed by patterning and etching the terminal metal layer used to form a die active area. The locking structures adhere to the overlying passivation and prevent its delamination by providing increased surface area for adherence.

DETAILED DESCRIPTION - **Integrated circuit** comprises in order: silicon substrate; a number of **dielectric** and metal **layers** forming a die active area, the metal layers having a guard wall surrounding the die active area and the metal layers having a segmented guard wall surrounding the first guard wall and stapling the metal layers. A passivation layer adheres to the first and the segmented guard wall.

USE - Fabrication of **integrated circuits**.

ADVANTAGE - The structure reduces the possibility of sawing cuts through the guard wall and prevents interlayer delamination.

DESCRIPTION OF DRAWING(S) - The drawing shows an **integrated**

circuit of the invention.
Die active area (501)
Terminal metal layer (502)
Guard ring (504)
Locking structures (506)
Guard wall (508)
Lateral surfaces (511)
Top surface (531)
Metal **layers** with interposed **dielectric layers** (M1 - M5)
pp; 32 DwgNo 6/12

11/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012398016
WPI Acc No: 1999-204123/199917
XRAM Acc No: C99-059418
XRPX Acc No: N99-150326
Integrated circuit (**IC**) with energy absorbing structure
Patent Assignee: INTEL CORP (ITLC)
Inventor: HICKS J M; **SESHAN K**
Number of Countries: 083 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5880528	A	19990309	US 97940439	A	19970930	199917	B
WO 9917362	A1	19990408	WO 98US13568	A	19980629	199921	
AU 9883784	A	19990423	AU 9883784	A	19980629	199935	
GB 2345579	A	20000712	WO 98US13568	A	19980629	200035	
			GB 20007668	A	20000329		
TW 432635	A	20010501	TW 98111406	A	19980714	200168	
GB 2345579	B	20020814	WO 98US13568	A	19980629	200261	
			GB 20007668	A	20000329		

Priority Applications (No Type Date): US 97940439 A 19970930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5880528	A		17	H01L-023/48	
WO 9917362	A1	E			

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9883784	A		Based on patent WO 9917362
GB 2345579	A	H01L-023/58	Based on patent WO 9917362
TW 432635	A	H01L-021/822	
GB 2345579	B	H01L-023/58	Based on patent WO 9917362

Abstract (Basic): US 5880528 A
Abstract (Basic):
NOVELTY - The **IC** has a terminal metal layer forming guards rings enclosing a die active area.
DETAILED DESCRIPTION - The **IC** comprises a silicon substrate, a **dielectric layer** and a terminal metal **layer** (TML).

The **dielectric layer** and the TML form a die active region enclosed by first and second guard ring formed from the TML.

USE - Used to provide ICs with structures that reduce or prevent damage.

DESCRIPTION OF DRAWING(S) - The drawing shows a top view of a wafer that includes four adjacent **chips**.

Wafer ((800))
Die active areas ((801)
ICs ((802))
Guard rings ((808,811)
pp; 17 DwgNo 8/12

11/3,AB/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011223571
WPI Acc No: 1997-201496/199718
Related WPI Acc No: 1995-302199
XRPX Acc No: N97-166602

Programmable fuse manufacture for **integrated circuit** on insulating substrate - using thermally linked primary and secondary fuses with different lengths and primary fuse at greater temperature than secondary in normal operation

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: BEZAMA R J; SCHEPIS D J; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5614440	A	19970325	US 94292901	A	19940810	199718	B
			US 95419778	A	19950411		

Priority Applications (No Type Date): US 94292901 A 19940810; US 95419778 A 19950411
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5614440	A		9	H01L-021/44	Div ex application US 94292901
					Div ex patent US 5444287

Abstract (Basic): US 5614440 A

The method includes the steps of forming a pair of current carrying fuse links (25,27) on the **insulating layer**, with the links in close proximity, coplanar and parallel to each other. One of the fuse links is a heating element. A portion of the pair of fuse links are thermally coupled with thermally conductive, electrically insulating material (10).

One link of the pair is programmed by activating the second link of said pair to transfer energy from the second fuse link to the first link of said pair via the thermally conductive material. An **insulating layer** is deposited over the pair of fuse links and thermally conductive material. Each link of the pair of current carrying fuse links has two terminals (20,22) attached to an interconnecting wire that provides wiring to the **integrated circuit**.

ADVANTAGE - Immunity to electrical noise causing accidental programming. Programming using relatively low current. Compatible with standard CMOS fabrication techniques. Minimal debris creation during

blow phase. Scalable structure. Programmable after **IC chip** has been mounted on next level of assembly.
Dwg.3/4

11/3,AB/9 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010587456
WPI Acc No: 1996-084409/199609
XRAM Acc No: C96-027304
XRPX Acc No: N96-070775
Programmable self cooling type electrical fuse for VLSI circuit - has heat conduction **layer** provided on third **insulation layer** that dissipates heat generated by fuse links
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: BEZAMA R J; SCHEPIS D J; **SESHAN K**
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7335761	A	19951222	JP 95135339	A	19950601	199609	B
US 5585663	A	19961217	US 94258162	A	19940610	199705	
			US 95511565	A	19950804		
US 5622892	A	19970422	US 94258162	A	19940610	199722	
			US 95407431	A	19950317		

Priority Applications (No Type Date): US 94258162 A 19940610; US 95511565 A 19950804; US 95407431 A 19950317
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7335761	A		8	H01L-021/82	
US 5585663	A		8	H01L-029/00	Cont of application US 94258162
US 5622892	A		8	H01L-021/306	Div ex application US 94258162

Abstract (Basic): JP 7335761 A
The fuse has a first **insulation layer** formed on a substrate (1). A number of conductors are formed on the **insulation layer** (13) and every two conductors are linked. The links or programme such that they are cut on excess conditions. The conductors and the links are covered by a second **insulation layer**. A heat conduction layer is provided on a third **insulation layer** to dissipate heat generated by the fuse links.
ADVANTAGE - Protects surrounding layer of fuse.
Dwg.1/7
Abstract (Equivalent): US 5622892 A
A method **of making** a buried semiconductor fuse structure in an **integrated circuit** comprising: forming **a first insulating layer** on a substrate having conductive lines formed thereon; forming a fuse link comprising a narrow strip having a conductive pad attached at each end, the fuse link connecting at least two of the conductive lines, the fuse link programmed to blow; forming at least one second **insulating layer** on the conductive lines and the fuse link; forming a thermally conductive **layer** on the second **insulating layer** and completely covering the fuse link, the thermally conductive layer dissipating heat developed during programming of the

fuse link; and providing at least one third insulating **layer** formed on **the thermally** conductive **layer**, wherein the thermally conductive layer shields the conductive lines and **the** third **insulating layer** from excessive thermal energy generated during the **programming of** the fuse link.

Dwg.3/4

US 5585663 A

In an **integrated circuit**, a buried semiconductor fuse structure comprising: a first electrical and thermal **insulating layer** formed on a substrate and having conductive lines formed on it; a fuse link comprising a narrow strip and a contact positioned at each end of the narrow strip, each the contacts connecting at least one of the conductive lines;

at least one second electrical and thermal **insulating layer** on the conductive lines and on the fuse link; a thermally conductive layer formed on the at least one second electrical and thermal **insulating layer** and covering the fuse link, the thermally conductive layer dissipating heat developed during electrical programming of the fuse link; and at least one electrical **insulating layer** formed on the thermally conductive layer and covering the fuse link, where the thermally conductive layer shields the at least one electrical **insulating layer** from excessive thermal energy generated within the fuse link during the electrical programming of the fuse.

Dwg.3b/7

11/3,AB/10 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

010400886
WPI Acc No: 1995-302199/199539
Related WPI Acc No: 1997-201496
XRPX Acc No: N95-229423

Electrically programmable noise-immune fuse structure in **integrated circuit** with insulated substrate - includes two adjacent fuse links on **insulating layer**, coupled by thermally conductive material, and has voltage pulses applied to links so that heat is transferred from primary link to secondary link

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: BEZAMA R J; SCHEPIS D J; **SESHAN K**
Number of Countries: 007 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5444287	A	19950822	US 94292901	A	19940810	199539	B
EP 696812	A1	19960214	EP 95480092	A	19950713	199611	
JP 8064105	A	19960308	JP 95177357	A	19950713	199620	
CN 1120735	A	19960417	CN 95109902	A	19950707	199745	
KR 157348	B1	19981116	KR 9524517	A	19950809	200030	
JP 3065512	B2	20000717	JP 95177357	A	19950713	200039	

Priority Applications (No Type Date): US 94292901 A 19940810
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5444287	A		11	H01L-029/167	
EP 696812	A1	E	9	H01H-085/046	
Designated States (Regional): DE FR GB					
JP 8064105	A		9	H01H-085/00	

CN 1120735 A H01L-023/52
KR 157348 B1 H01H-085/00
JP 3065512 B2 9 H01H-085/00 Previous Publ. patent JP 8064105

Abstract (Basic): US 5444287 A

The **IC** programmable fuse structure has sub-micron dimensions and can be programmed by electrically and thermally synchronized pulses. The fuse includes a pair of fuse links close to each other on an **insulating layer** in the **IC**, with a layer of thermally conductive and electrically insulating material thermally coupling and extending partly over the two links. The first link of the pair is programmed by prompting the second link in the pair to gate an energy transfer between the links through the coupling layer.

Pref. the substrate is **insulated** by a **layer** of SiO2 formed on the substrate. Pref. each link of the pair has two terminals, each terminal respectively attached to an interconnecting wire in the **IC**, with one terminal of each fuse sharing a common interconnecting line. A programming voltage pulse may be applied simultaneously to each link of the pair of fuse links.

USE/ADVANTAGE - Field programming e.g. for redundancy. Improved reliability compared to single fuse link element; programmed at low current; CMOS and BiCMOS process compatible; minimises debris during programming

Dwg.3/6

11/3,AB/11 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008945075
WPI Acc No: 1992-072344/199209
XRAM Acc No: C92-033244
XRPX Acc No: N92-054335
Misalignment tolerant anti-fuse - has reduced susceptibility to misalignment of the mask layers used to form its features
Patent Assignee: ACTEL CORP (ACTE-N); ACTEL CORP US (ACTE-N)
Inventor: **BAKKER G W**; CHEN S O; CHIANG S S
Number of Countries: 015 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5087958	A	19920211	US 90609177	A	19901105	199209	B
EP 489488	A2	19920610	EP 91309178	A	19911007	199224	
JP 4284649	A	19921009	JP 91317571	A	19911105	199247	
EP 489488	A3	19920701	EP 91309178	A	19911007	199333	

Priority Applications (No Type Date): US 90609177 A 19901105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 489488	A2	E	10	H01L-023/525	
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
JP 4284649	A		16	H01L-021/82	

Abstract (Basic): US 5087958 A

An antifuse includes a lower electrode with 2 opposing sides; a **dielectric layer** on the surface of the lower electrode; a pair of regions in the **dielectric layer**, one each of the pair of regions abuting the 2 opposing sides of the lower electrode,

the regions have a thickness less than the thickness of the remainder of the **dielectric layer**, the regions have a total area below 0.7 square microns; an upper electrode disposed above the **dielectric layer** and lying over the pair of regions. Pref. the lower electrode comprises a doped region in a semiconductor substrate, bounded on at least the first and second opposing sides by field oxide regions; the upper electrode is heavily doped polysilicon or a metal; the **dielectric layer** is SiO2 and/or Si3N4.

USE/ADVANTAGE - An antifuse which has a reduced suseptability to misalignment of the mask layers which are used to form its features during semiconductor **IC** fabrication. (9pp Dwg.No.2d/6)

13/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5534462 INSPEC Abstract Number: B9705-2550E-058
Title: Removal of thermally grown **silicon dioxide** films using water at elevated temperature and pressure
Author(s): **Bakker, G.L.**; Hess, D.W.
Author Affiliation: Dept. of Chem. Eng., Lehigh Univ., Bethlehem, PA, USA
Conference Title: Proceedings of the Fourth International Symposium on Cleaning Technology in Semiconductor Device Manufacturing p.464-71
Editor(s): Novak, R.E.; Ruzyllo, J.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1996 Country of Publication: USA xii+626 pp.
Material Identity Number: XX97-00338
Conference Title: Proceedings of the Fourth International Symposium on Cleaning Technology in Semiconductor Device Manufacturing
Conference Date: Oct. 1995 Conference Location: Chicago, IL, USA
Language: English
Abstract: The removal of thermally grown **silicon dioxide** films from **silicon** wafer surfaces with water at elevated temperature and pressure was studied using ellipsometry and X-ray photoelectron spectroscopy (XPS). Complete removal of 50 nm **silicon dioxide** layers was observed with XPS after exposure of the sample to de-ionized (18 M Omega -cm) water at 280 degrees C and 241 bar (3500 psi) for 30 minutes. To the detection limit of XPS (~0.5 atomic percent), no metal contamination was deposited on the surface. Removal rates were determined at temperatures between 260 degrees C and 305 degrees C at 138 bar (2000 psi). A surface reaction limited rate equation, used previously to describe quartz dissolution in water over a wide range of temperature, was used to estimate rate constants for **silicon dioxide** removal. An effective activation energy of 76.6 kJ/mol was calculated for the etching process, which is comparable to values reported for quartz dissolution under similar conditions (62.6-79.0 kJ/mol).
Subfile: B

15/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013144897
WPI Acc No: 2000-316769/200027
XRAM Acc No: C00-095704
XRPX Acc No: N00-237763
Passivating **integrated circuit** comprises depositing silicon nitride over a top surface portion of the circuit, and treating the exposed surface to form **silicon oxynitride**
Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; GAETA I; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6046101	A	20000404	US 971970	A	19971231	200027	B

Priority Applications (No Type Date): US 971970 A 19971231
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6046101	A		13	H01L-021/318	

Abstract (Basic): US 6046101 A
Abstract (Basic):
NOVELTY - **Integrated circuit** is passivated by depositing a silicon nitride layer over the top surface of a portion of an **integrated circuit**, treating an exposed surface of the first passivation layer to form a **silicon oxynitride** layer and depositing a second passivation layer over the first passivation layer.
USE - For passivating **integrated circuit**.
ADVANTAGE - Delamination is minimized by eliminating passivation material from the scribe street area prior to separating devices and the combined passivation technology has robust passivation resistance to thin film delamination.
pp; 13 DwgNo 0/21

```
   25aug03 10:08:38 User267149 Session D941.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2003/Aug W2
         (c) 2003 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2003/Aug W4
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
*File   6: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   8:Ei Compendex(R)  1970-2003/Aug W3
         (c) 2003 Elsevier Eng.  Info. Inc.
*File   8: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File  34:SciSearch(R) Cited Ref Sci  1990-2003/Aug W3
         (c) 2003 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2003/Jul
         (c) 2003 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2003/Aug W3
         (c) 2003 BLDSC all rts. reserv.
  File  94:JICST-EPlus  1985-2003/Aug W4
         (c)2003 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2003/Jul
         (c) 2003 The HW Wilson Co.
  File 144:Pascal  1973-2003/Aug W2
         (c) 2003 INIST/CNRS
  File 305:Analytical Abstracts  1980-2003/Jul W4
         (c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2003/Jul
         (c) 2003 DECHEMA
  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200354
         (c) 2003  Thomson Derwent
  File 347:JAPIO  Oct 1976-2003/Apr(Updated 030804)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2003/Mar
         (c) 2003 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

Set	Items	Description
S1	1329852	(INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?)) OR IC OR CHIP? ?
S2	190013	CLOS????????(3N)(CIRCUIT???????? OR LOOP? ? OR PATH? ? OR ROUTE? ? OR ELECTRODE? ?)
S3	24382	MC=(U11-D01A OR U13-D02 OR U13-D02A)
S4	1528236	S1:S3
S5	3048	OXYD????????(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S6	470630	(INSULAT???????? OR DIELECTR????????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S7	207906	(SILICON OR SI)(3N)DIOXIDE OR SIO2
S8	451819	(ADHESIVE? ? OR ADHERE??? OR ATTACH??????? OR SECUR??????? OR CONNECT???????? OR STICK???????? OR SEAL????????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER???? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER???...
S9	12814	(SILICON OR SI)(3N)OXYNITRIDE OR SION
S10	1654822	(PASSIVAT???????? OR COAT?????? OR TREAT??????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S11	25	(PHOTODEFIN???????? OR PHOTO()DEFIN????????)(3N)(PASSIVAT??????? OR COAT?????? OR TREAT??????)
S12	29219	(SOFT OR HARD)(3N)(PASSIVAT???????? OR COAT?????? OR TREAT???)
S13	119125	(SILICON OR SI)(3N)NITRIDE OR SI3N4
S14	1764994	S10:S13
S15	36	S4 AND S5
S16	6	S15 AND S6
S17	6	RD (unique items)
S18	30	S15 NOT S16
S19	1	S18 AND S7
S20	29	S18 NOT S19
S21	0	S20 AND S8
S22	0	S20 AND S9
S23	7	S20 AND S14
S24	4	RD (unique items)
S25	22	S20 NOT S23
S26	0	S25 AND S13
S27	10027	S1 AND S7
S28	218	S27 AND S9
S29	163	S28 AND S13
S30	163	S29 AND S14
S31	105	S30 AND S6
S32	4	S31 AND S8
S33	4	RD (unique items)
S34	101	S31 NOT S32
S35	0	S34 AND S5
S36	101	S34 AND S1
S37	26	S36 AND S10
S38	0	S37 AND S11
S39	2	S37 AND S12
S40	2	RD (unique items)

S41	24	S37 NOT S39
S42	24	RD (unique items)

17/3,AB/1 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15423005 PASCAL No.: 02-0114660

Optimization of tribological properties of silicon dioxide during the chemical mechanical planarization process

SIKDER A K; GIGLIO Frank; WOOD John; KUMAB Ashok; ANTHONY Mark

Center for Microelectronics Research, College of Engineering, University of South Florida, Tampa, FL 33620, United States; Department of Mechanical Engineering, University of South Florida, United States

International Technology Roadmap for Semiconductors (ITRS). Symposium, 1 (New Orleans USA) 2001-02

Journal: Journal of electronic materials, 2001, 30 (12) 1520-1526

Language: English

Chemical mechanical planarization (CMP) has been proved to achieve excellent global and local planarity, and, as feature sizes shrink, the use of CMP will be critical for planarizing multilevel structures. Understanding the tribological properties of a **dielectric layer** in the CMP process is critical for successful evaluation and implementation of the materials. In this paper, we present the tribological properties of silicon dioxide during the CMP process. A CMP tester was used to study the fundamental aspects of the CMP process. The accessories of the CMP tester were first optimized for the reproducibility of the results. The coefficient of friction (COF) was measured during the process and was found to decrease with both down pressure and platen rotation. An acoustic sensor attached to this tester is used to detect endpoint, delamination, and uniformity. The effects of machine parameters on the polishing performance and the correlation of physical phenomena with the process have been discussed.

17/3,AB/2 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

15130668 PASCAL No.: 01-0293203
Optimization of sub-5-nm multiple-thickness gate oxide formed by oxygen implantation
KING Y C; KUO C; KING T J; HU C
Department of Electrical Engineering National Hsinghua University, Hsinchu 30043, Taiwan
Journal: IEEE Transactions on Electron Devices, 2001, 48 (6) 1279-1281
Language: English
A new method of growing multiple gate oxide thicknesses below 5 nm using masked oxygen implantation is presented. Multiple thicknesses can be achieved on the same wafer without degradation in the oxide properties. The oxygen implanted oxide quality is comparable to that of thermally grown oxides. Moreover, the effects of oxygen implant damage is minimized with higher implant energies, thicker sacrificial oxides, and low-temperature annealing.

17/3,AB/3 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

12920909 PASCAL No.: 97-0189438
Deuterium post-metal annealing of MOSFET's for improved hot carrier reliability
KIZILYALLI I C; LYDING J W; HESS K
Bell Lab, Orlando FL, United States
Journal: IEEE Electron Device Letters, 1997, 18 (3) 81-83
Language: English
Low-temperature post-metallization anneals in hydrogen ambients are critical to CMOS fabrication technologies in reducing Si/SiO SUB 2 interface trap charge densities by hydrogen passivation. In this letter we show that the hot carrier reliability (lifetime) of NMOS transistors can be increased by an order of magnitude when wafers are annealed in a deuterium ambient. This phenomenon can be understood as a kinetic isotope effect. The chemical reaction rates involving the heavier isotopes are reduced, and consequently, under hot electron stress, bonds to deuterium are more difficult to break than bonds to protium (H). However, the static chemical bonding (i.e., binding energies and excited states) is evidently the same for both hydrogen and deuterium. We measure identical transistor function after hydrogen and deuterium treatment before hot electron dynamics and resultant damage. Therefore, deuterium and hydrogen post-metal anneal processes are compatible with each other in semiconductor manufacturing. SIMS analysis proves that at typical anneal temperatures (400-450 Degree C), deuterium diffuses rapidly through the interlevel oxides and accumulates at Si/SiO SUB 2 interfaces. Transistor speed versus reliability trade-off in CMOS device design is discussed in light of the findings of this study.

17/3,AB/4 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal

08686569 PASCAL No.: 89-0235822
Mise au point et optimisation d'un equipement industriel de depots chimiques en phase vapeur actives par plasma (PACVD)
(Development and optimization of an industrial equipment for plasma activated chemical vapor deposition (PACVD))
LAPARRA Olivier; LECOY Gilles, Dir the
Univ.: Montpellier 2 Degree: Th. doct. : Compos. signal syst.
1987; 1987 161 p.
Language: French

La technique de depots chimiques en phase activites par plasma a connu au cours de ces dernieres annees un developpement important. Notre travail a consiste a mettre au point un equipement industriel de depots assistes par plasma et a en optimiser les performances. Au cours de cette etude ont ete realises des depots de **films dielectriques** (**oxydes**, nitrures...) utilises lors de l'elaboration des circuits integres. Une analyse systematique des differents parametres de depots (temperature, pression, melanges gazeux, puissance de plasma, positionnement des plaquettes, etc...) intervenant lors des processus technologiques est presentee dans ce memoire

17/3,AB/5 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009082071
WPI Acc No: 1992-209487/199226
XRAM Acc No: C92-095044
XRPX Acc No: N92-158875
Tetrapolyimide **film** contg. **oxydiphthalic** dianhydride - having low water absorption, low coefficient of thermal and hygroscopic expansion
Patent Assignee: DU PONT DE NEMOURS & CO E I (DUPO)
Inventor: KREUZ J A
Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 491308	A1	19920624	EP 91121487	A	19911214	199226	B
CA 2057420	A	19920618	CA 2057420	A	19911211	199236	
JP 4293937	A	19921019	JP 91331948	A	19911216	199248	
US 5219977	A	19930615	US 90628233	A	19901217	199325	
			US 92920690	A	19920730		
EP 491308	B1	19960911	EP 91121487	A	19911214	199641	
DE 69122063	E	19961017	DE 622063	A	19911214	199647	
			EP 91121487	A	19911214		
JP 3256252	B2	20020212	JP 91331948	A	19911216	200213	

Priority Applications (No Type Date): US 90628233 A 19901217; US 92920690 A 19920730
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 491308	A1	E	11	C08G-073/10	
Designated States (Regional): DE FR GB IT					
CA 2057420	A			C08G-073/10	
JP 4293937	A		8	C08J-005/18	
US 5219977	A			C08G-073/10	Cont of application US 90628233
EP 491308	B1	E	12	C08G-073/10	
Designated States (Regional): DE FR GB IT					
DE 69122063	E			C08G-073/10	Based on patent EP 491308
JP 3256252	B2		8	C08J-005/18	Previous Publ. patent JP 4293937

Abstract (Basic): EP 491308 A

A tetrapolyimide **film** for **dielectric** use in flexible printed circuits and tape automated bonding applications comprises on the basis of dianhydride 20-70 (pref. 30-70 esp. 60) mole % oxydiphthalic dianhydride (ODPA) and 30-80 (pref. 30-70 esp. 40) mole % pyromellitic acid dianhydride (PMDA) and, on the basis of diamine 30-80 (pref. 50-80 esp. 70) mole % of a (pref. p-) phenylene diamine (PPD) and 20-70 (pref. 20-50 esp. 30) mole % of a (pref. 4,4'-) diaminophenyl ether (ODA).

Also claimed are a chemical conversion process for forming the film and a film so prepd. having an elastic modulus of 400-1000 Kpsi, coefft. of thermal expansion 8-35 ppm./deg.C, coefft. of hygroscopic expansion 10-30/ppm.% RH, water absorption less than 4% and an etch rate greater than the same tetrapolyimide film prepd. by a thermal conversion process using the same time and temp. conditions.

USE/ADVANTAGE - The tetrapolymer films have low water absorption, low thermal and hygroscopic expansion coeffts. and high modulus, and

are caustic etchable and are used e.g. in TAB **chip** packaging technologies and flexible printed circui

Dwg.0/0

Abstract (Equivalent): EP 491308 B

A chemically converted tetrapolyimide film derived from two tetracarboxylic dianhydrides and two diamines for use as a dielectric in flexible printed circuits and tape automated bonding applications comprising on the basis of dianhydride from 20 to 70 mole% of oxydiphthalic dianhydride and from 30 to 80 mole% of pyromellitic acid dianhydride and on the basis of diamine from 30 to 80 mole% of a phenylene diamine and from 20 to 70 mole% of a diaminodiphenyl ether, said tetrapolyimide film being obtained by a process comprising the steps of: (a) reacting substantially equimolar amounts of oxydiphthalic dianhydride, pyromellitic acid dianhydride, a phenylene diamine, and a diaminodiphenyl ether in an inert organic solvent selected from N-methyl-2-pyrrolidone, dimethylsulphoxide, N,N-dimethylacetamide, N,N-diethyl-formamide, N,N-diethylacetamide, N,N-dimethyl-formamide and mixtures thereof for a sufficient time and at a temperature below 175 deg.C sufficient to form a tetrapolyimide acid solution containing from 5 to 40 weight% of tetrapolyamide acid polymer in said solvent; (b) mixing said tetrapolyamide acid solution with from 2 to 2.4 molar equivalents of tertiary amine catalysts and anhydride dehydrating materials for converting the tetrapolyamide acid to tetrapolyimide; (c) casting or extruding the mixture from step (b) onto a heated conversion surface of a temperature between 15 deg. and 120 deg.C to form a tetrapolyamide acid-tetrapolyimide gel film; or alternatively in place of steps (b) and (c) a single step of casting or extruding said tetrapolyamide acid solution into a mixture or solution of from 2 to 2.4 molar equivalents of tertiary amine catalysts and anhydride dehydrating materials for converting the tetrapolyamide acid to a tetrapolyamide acid-tetrapolyimide gel film; and (d) heating said gel film from step (c) at a temperature and for a time sufficient to convert said tetrapolyamide acid to tetrapolyimide.

(Dwg.0/0)

Abstract (Equivalent): US 5219977 A

A chemically converted tetrapolyimide film comprises 20-70 wt.% of oxydiphthalic dianhydride, and 30-80 mol.% of pyromellitic acid dianhydride and 30-80 mol.% of a phenylene diamine and 20-70 mol.% of a diaminodiphenylether. The tetrapolyimide film has an elastic modulus of 400-1000 Kpsi, a coefft. of thermal expansion of 8-35 ppm/dec.C, a coefft. of hygroscopic expansion of 10-30 ppm/% RH, a water absorption of less than 4% and an etch rate greater than the same tetrapolyimide film prepd. by a thermal conversion process using the same time and temp. conditions.

USE/ADVANTAGE - Used for dielectric use in flexible printed circuits and tape onto metal bonding application. The films have low water absorption, low coefft. of thermal and hygroscopic expansion and are caustic etchable.

Dwg.0/0

17/3,AB/6 (Item 1 from file: 371)
000868816
Title: Condensateur a constante dielectrique elevee et procede pour sa fabrication.
Patent Applicant/Assignee: SAMSUNG ELECTRONICS CO LTD
Applicant Address: SOCIETE DITE : SAMSUNG ELECTRONICS CO., LTD.- Deposant - 416, MAETAN 3-DONG, KWONSUN-KU, SUWON KYUNGKI-DO REPUBLIQUE DE COREE (KR)
Inventor(s): KWON KEEWON - N 106-304, DONGSHIN APT., 401, JEONGJA-DONG, CHANGAN-KU SUWON, KYUNGKI-DO REPUBLIQUE DE COREE (KR); KIM YOUNGWUG - N 102-307, HANSHIN APT., INKEI-DONG, KWONSUN-KU SUWON, KYUNGKI-DO REPUBLIQUE DE COREE
Legal Representative: CABINET LAVOIX
Document Type: Patent / Brevet
Patent and Priority Information (Country, Number, Date):
Patent: FR 2678766 - 19930108
Application: FR 928264 - 19920703
Priority Application: KR 9111272 - 19910703

Abstract:
Film a constante **dielectrique** elevee compose d'au moins une couche de film double, qui comprend un premier **film** d'**oxyde** de tantale (3), et un premier **film** d'**oxyde** metallique (4) qui est fait d'un oxyde metallique dont la valence est plus faible que celle du tantale, et dont la constante dielectrique est egale ou superieure a celle de l'oxyde de tantale. Le premier **film** d'**oxyde** metallique (4) a de preference une epaisseur inferieure a 50 A environ. Le premier **film** d'**oxyde** de tantale (3) a de preference une epaisseur dans la gamme allant de 5 A environ a 200 A environ, le rapport entre l'epaisseur du premier **film** d'**oxyde** de tantale et l'epaisseur du premier **film** d'**oxyde** metallique se situant dans la gamme allant de 1:10 a 100:1.

Legal Status (Type, Action Date, BOPI No, Description):
Publication 19930108 9301 Date published
Search Report 19930402 9313 Date Search Report published
Rejected Rejected

19/3,AB/1 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

12868859 PASCAL No.: 97-0128054
Etude de la stabilite mecanique de films de passivation destines a la microelectronique
(Study of the mechanical stability of passivation films used in microelectronics)
SCAFIDI Pascal; IGNAT M, dir
Institut national polytechnique de Grenoble, Grenoble, Francee
Univ.: Institut national polytechnique de Grenoble. Grenoble. FRA
Degree: Th. doct.
1995-05; 1995 188 p.
Language: French Summary Language: French; English
La stabilite mecanique de **films** minces d'**oxyde** de silicium dope au phosphore et de nitrure de silicium est etudiee a partir d'une methodologie experimentale basee sur la realisation d'essais micro-mecaniques, associee a l'observation, a l'analyse et a la modelisation des endommagements induits. Nous considerons des systemes film/substrat et des systemes multicouches. Par indentation submicronique, nous determinons la durete et le module elastique des films etudies. Leur contrainte residuelle est ensuite evaluee a partir de mesures de courbures. Lors de la sollicitation en traction in situ de chaque systeme film/substrat dans un microscope electronique a balayage, la fissuration transversale du film precede son decollement et son flambement. L'analyse de ces endommagements par des modeles de la mecanique de la rupture permet de determiner les energies de fissuration et les tenacites des films et des interfaces. En complement, des experiences de traction in situ dans un microscope acoustique sont realisees. La vitesse de propagation des ondes acoustiques de surface constitue un parametre adapte a la caracterisation de l'evolution de l'endommagement. La stabilite mecanique des films presents dans les systemes multicouches est analysee a partir de deux essais mecaniques: l'indentation submicronique et la flexion cyclique quatre points. Pour ce dernier essai, l'amorcage de l'endommagement des films, prevu par des modelisations numeriques par elements finis, est revele par imagerie acoustique et par la variation de la vitesse des ondes acoustiques de surface

24/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5727302 INSPEC Abstract Number: A9723-8245-007, B9712-0560-001
Title: Evaluation of polyimide coatings integrity by positron annihilation lifetime spectroscopy and electrochemical impedance spectroscopy
Author(s): Madani, M.M.; Vedage, H.L.; Granata, R.D.
Author Affiliation: Zettlemoyer Center for Surface Studies, Lehigh Univ., Bethlehem, PA, USA
Journal: Journal of the Electrochemical Society vol.144, no.9 p. 3293-8
Publisher: Electrochem. Soc,
Publication Date: Sept. 1997 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(199709)144:9L.3293:EPCI;1-4
Material Identity Number: J010-97010
U.S. Copyright Clearance Center Code: 0013-4651/97/$7.00
Language: English
Abstract: Positron annihilation lifetime spectroscopy (PALS) and electrochemical impedance spectroscopy (EIS) were used to investigate the existence of free volume cavities in polyimide coatings and the durability of these films for **integrated circuits**, as a function of their curing temperature. Impedance of the coatings vs. resistance to water uptake in the films was measured by EIS. A several orders of magnitude increase in the low frequency electrochemical impedance was observed for polyimide PI2566 (2,2'bis(3,4-dicarboxyphenyl) hexafluoroisopropylidene dianhydride+4,4' **oxydianiline**) when the **coating** was cured at increasing temperatures. Water exposure decreases the low frequency impedance, indicating water penetrates and changes the dielectric and conduction properties of the film. PI2566 cured above 150 degrees C was resistant to diffusion of water after 900 h exposure. PALS showed the free volume fraction in PI2566 increased approximately 35% as a function of its curing temperature. PALS data showed three lifetimes and intensities in the polyimide specimens. There were three curing temperature regions in the free volume fraction and the average lifetime data corresponded to three imidization stages. The first region was associated with the evaporation of solvent. The second region was due to the condensation reaction (loss of water from the polyimide). A third region was related to completion of imidization. The free volume cavities increased from 46 AA/sup 3/ to 148 AA/sup 3/ with increasing curing temperature for PI2566. No large free volume cavities were found in PI2610D polyimide (pyromellitic dianhydride+oxydianiline) at curing temperatures above 150 degrees C.
Subfile: A B

24/3,AB/2 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

12440386 PASCAL No.: 96-0096871
Formation of metal oxides by cathodic arc deposition
ANDERS S; ANDERS A; RUBIN M; WANG Z; RAOUX S; KONG F; BROWN I G
JEHN Hermann A, ed; MATTHEWS Allan, ed; MCGUIRE Gary E, ed; PETROV Ivan, ed
Univ. California, Lawrence Berkeley lab., Berkeley CA 94720, USA
Forschungsinst. Edelmetalle Metallchemie, 73525 Schwaebisch Gmuend, Federal Republic of Germany
American Vacuum Society. vacuum metallurgy and thin films division, New York NY, USA.
International conference on metallurgical coatings and thin films ICMCTF95, 22 (San Diego CA USA) 1995-04-24
Journal: Surface & coatings technology, 1995, 76-77 (1-3 p.1) 167-173
Language: English
Cathodic arc deposition is an established and industrially applied technique for the formation of nitrides (e.g. TiN) ; it can also be used for metal oxide thin film formation. A cathodic arc plasma source with the desired cathode material is operated in an oxygen atmosphere of appropriate pressure, and metal oxides of various stoichiometric composition can be formed on different substrates. We report here on a series of experiments on metal oxide formation by cathodic arc deposition for different applications. Black copper oxide has been deposited on accelerator components to increase the radiative heat transfer between the parts. Various metal oxides such as tungsten oxide, niobium oxide, nickel oxide and vanadium oxide have been deposited on ITO glass to form electrochromic films for window applications. Optical waveguide structures can be formed by refractive index variation using oxide multilayers. We have synthesized multilayers of Al SUB 2 O SUB 3 -Y SUB 2 O SUB 3 -Al SUB 2 O SUB 3 -Si as possible basic structures for passive optoelectronic **integrated circuits**, and Al SUB 2 SUB - SUB x Er SUB x B SUB 3 thin films with a variable Er concentration which is a potential component layer for the production of active optoelectronic integrated devices such as amplifiers or lasers at a wavelength of 1.53 mu m. Aluminum and chromium oxide films have been deposited on a number of substrates to impart improved corrosion resistance at high temperature. Titanium sub-oxides which are electrically conductive and corrosion resistant and stable in a number of aggressive environments have been deposited on various substrates. These sub-oxides are of great interest for use in electrochemical cells. Common features of all these depositions are the high deposition rate typical for cathodic arc deposition, the good adhesion of the films due to the high metal ion energy, and the advantage of an environmentally clean method in comparison to wet-chemical oxide formation techniques.

24/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014572959
WPI Acc No: 2002-393663/200242
XRAM Acc No: C02-110665
XRPX Acc No: N02-308669
Polyimide film used as metal inter-connection board substrate, is manufactured from polyamic acid prepared from pyromellitic dianhydride in combination with preset amount of phenylenediamine and 3,4'-oxydianiline
Patent Assignee: DU PONT DE NEMOURS & CO E I (DUPO); DU PONT TORAY CO LTD (DUPO)
Inventor: AUMAN B C; SAWASAKI K; SUMMERS J D; UHARA K; YASUDA N
Number of Countries: 098 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200216475	A2	20020228	WO 2001US26289	A	20010823	200242	B
AU 200185217	A	20020304	AU 200185217	A	20010823	200247	
JP 2002138152	A	20020514	JP 2001251557	A	20010822	200247	
EP 1313795	A2	20030528	EP 2001964353	A	20010823	200336	
			WO 2001US26289	A	20010823		

Priority Applications (No Type Date): JP 2001251557 A 20010822; JP 2000253420 A 20000824
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200216475	A2	E	23	C08G-073/10	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200185217	A			C08G-073/10	Based on patent WO 200216475
JP 2002138152	A		13	C08J-005/18	
EP 1313795	A2	E		C08G-073/10	Based on patent WO 200216475

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): WO 200216475 A2
Abstract (Basic):
NOVELTY - A polyimide film is manufactured from a polyamic acid prepared from pyromellitic dianhydride in combination with 10-60 mol% of phenylenediamine and 40-90 mol% of 3,4'-oxydianiline, based on total diamine.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(i) a method for manufacturing the polyimide film, which involves
(A) reacting starting material comprising (a1) tetracarboxylic acid dianhydride containing pyromellitic dianhydride and (b1) diamine (I), such as phenylenediamine and 3,4'-oxydianiline in an inert solvent to form a first polyamic acid solution containing components, such as block component and interpenetrating polymer network component of diamine (I) and pyromellitic dianhydride and an interpenetrating polymer network,
(B) adding first polyamic acid solution prepared in step (A)

additional material comprising (b1) tetracarboxylic acid dianhydride comprising pyromellitic dianhydride and (b2) diamine (II), such as phenylene diamine and 3,4'-oxydianiline, and continuing the reaction with all materials to form a second polyamic acid solution,

(C) mixing a chemical agent capable of converting the polyamic acid into polyimide, with second polyamic acid solution to form a mixture,

(D) casting or extruding the mixture into a smooth surface to form a polyamic acid-polyimide gel film, heating the gel film at 200-500degreesC to transform the polyamic acid to polyimide, where at least diamine (I) or diamine (II) is phenylene diamine or 3,4'-oxydianiline; and

(ii) a metal interconnect board substrate for use in flexible printed circuits or tape-automated bonding tape, formed by using the polyimide film as substrate and providing metal interconnection on the surface.

USE - Used as metal interconnection board substrate for flexible printed circuits and tape-automated bonding tape (claimed), **chip** scale packages, ball grid arrays for wiring electronic equipment.

ADVANTAGE - The polyimide film has high elastic modulus, low thermal expansion co-efficient, alkali etchability and excellent film-forming properties. The use of p-phenylenediamine increases the elastic modulus of the **film** and 3,4'-**oxydianiline** increases **film** elongation and improves film formability. An imidizing agent is mixed with polyamic acid and the solution is formed into a **film** then heat-**treated** to effect chemical conversion which leads to short imidization time, uniform imidization, easy peeling of the film from the support, and the ability to handle in closed system imidizing agent which has strong odor.

pp; 23 DwgNo 0/0

24/3,AB/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003286569
WPI Acc No: 1982-D4580E/198213
IC engine light metal cylinder head with embedded steel inserts - which have aluminium or ceramic **coating** for protection during anodising
Patent Assignee: KLOECKNER-HUMBOLDT-DEUTZ AG (KLOH)
Inventor: LICHTNER E
Number of Countries: 007 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 47835	A	19820324				198213	B
DE 3034591	A	19820429	DE 3034591	A	19800913	198218	
US 4426963	A	19840124	US 81298946	A	19810903	198406	
CA 1177348	A	19841106				198449	
DE 3034591	C	19851003				198541	

Priority Applications (No Type Date): DE 3034591 A 19800913
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 47835	A	G	10		

Designated States (Regional): AT DE FR GB IT

Abstract (Basic): EP 47835 A
An **IC** engine has a light alloy cylinder head (1) with holes (2,3) for inlet and outlet valves. The narrow bridge (5) between the valve holes is provided with expansion gaps (6,7) which are fitted with embedded strip steel inserts (8). The steel strips reduce the risk of cracks occurring as a result of thermal stresses in the cylinder head.
The risk of thermal stress cracks is further reduced by anodising the inside surface of the cylinder head so that an **oxydised film** is formed. In order to protect the steel inserts from attack by the acid of the anodising bath, they are first **coated** with aluminium or ceramics before being embedded in the aluminium cylinder head by casting.
1

33/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014414884
WPI Acc No: 2002-235587/200229
XRAM Acc No: C02-071480
XRPX Acc No: N02-180914
Metallization in production of **integrated circuit** device involves depositing oxide layer overlying polish stop layer
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: LIU C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6294457	B1	20010925	US 2001774418	A	20010201	200229	B

Priority Applications (No Type Date): US 2001774418 A 20010201
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6294457	B1		7	H01L-021/4763	

Abstract (Basic): US 6294457 B1
Abstract (Basic):

NOVELTY - Metallization in the production of an **integrated circuit** device involves depositing an oxide layer overlying a polish stop layer.

DETAILED DESCRIPTION - Metallization in the production of an **integrated circuit** device involves depositing an etch stop layer (16) overlying a semiconductor substrate. A low-**dielectric** constant material **layer** (18) is deposited overlying the etch stop layer. A polish stop layer (20) is deposited overlying the low-**dielectric** constant material **layer**. An oxide layer is deposited overlying the polish stop **layer**. An anti-reflective **coating** (ARC) **layer** is deposited overlying the oxide layer. An opening is etched through the ARC layer, oxide **layer**, polish stop **layer**, and low-**dielectric** constant material **layer** where they are not covered by a mask. The mask is removed during etching. The etch stop layer is etched through within the opening, removing the ARC layer. The opening is cleaned using an argon sputtering method, where particles from topmost **layer** **adhere** to walls of the sputtering chamber. The opening is filled with a metal layer (38) to complete metallization in the fabrication of an **integrated circuit** device.

USE - For metallization in the production of **integrated circuits**.

ADVANTAGE - The method avoids particle issue during pre-metal cleaning, thus improving yield in the manufacture of **integrated circuits**.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional representation of metallization in the production of **integrated circuit** devices.

Etch stop layer (16)
Low-**dielectric** constant material **layer** (18)
Polish stop layer (20)
Barrier metal layer (36)
Metal layer (38)

33/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013638283
WPI Acc No: 2001-122491/200113
XRAM Acc No: C01-035432
XRPX Acc No: N01-089948
Manufacture of **integrated circuit** involves etching **insulative layers** to a **dielectric**, and forming crossover, crossunder, or local interconnect in a different **connection layer**
Patent Assignee: VSLI TECHNOLOGY (VSLI-N)
Inventor: HARVEY I
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6174803	B1	20010116	US 98154050	A	19980916	200113	B

Priority Applications (No Type Date): US 98154050 A 19980916
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6174803	B1		26	H01L-021/4763	

Abstract (Basic): US 6174803 B1
Abstract (Basic):
NOVELTY - An **integrated circuit** is manufactured by selectively etching **insulative layers** to a **dielectric** included in the **connection layers**; and forming crossover, crossunder, or local interconnects (239c) in a different **connection layer** than the routing interconnects.
DETAILED DESCRIPTION - Manufacture of an **integrated circuit** (201) comprises providing electronic components along a semiconductor substrate, and a first **connection layer** (240) having a **dielectric** and conductors (293a-d) in contact with the components; and forming a first **insulative layer** on the first **connection layer** with a pattern of openings. A second **connection layer** (270) having **dielectric** (262, 272, 292) and conductors interconnecting the first conductors through the opening is established. A second **insulative layer** is formed on the second **connection layer** with a pattern of openings. A third **connection layer** (290) is formed on the second **insulative layer**. The third connection **layer** comprises a third **dielectric** and conductors interconnecting the second conductors, and is etched to the second **insulative layer**. The second and third conductors are in contact with the second **insulative layer**. The second conductor(s) crosses a third conductor(s), and is electrically isolated by the second **insulative layer**.
USE - None given.
ADVANTAGE - The method increases the density of **integrated circuit** component interconnects, improves circuit layout flexibility, and facilitates higher routing and interconnection density.
DESCRIPTION OF DRAWING(S) - The figure shows a partial, sectional side views of the **integrated circuit** device.

Integrated circuit (201)
Local interconnects (239c)
Connection layer (240)
Dielectric (262, 272, 292)
Connection layer (270, 290)
Recesses (292a-d)
Conductors (293a-d)
pp; 26 DwgNo 25/27

33/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012814634
WPI Acc No: 1999-620865/199953
XRAM Acc No: C99-181338
XRPX Acc No: N99-457921
Fabricating semiconductor **integrated circuit chip** structures for microprocessors and digital signal processors
Patent Assignee: CVC PROD INC (CVCC-N); CVC INC (CVCC-N)
Inventor: MOSLEHI M; MOSLEHI M M
Number of Countries: 021 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9954934	A1	19991028	WO 99US8475	A	19990422	199953	B
US 6016000	A	20000118	US 9864431	A	19980422	200011	
EP 1000440	A1	20000517	EP 99917606	A	19990422	200028	
			WO 99US8475	A	19990422		
US 6124198	A	20000926	US 9864431	A	19980422	200051	
			US 98187297	A	19981105		
KR 2001020476	A	20010315	KR 99712124	A	19991222	200159	
JP 2002506577	W	20020226	JP 99553180	A	19990422	200219	
			WO 99US8475	A	19990422		

Priority Applications (No Type Date): US 98187297 A 19981105; US 9864431 A 19980422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9954934	A1	E	78	H01L-023/48	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 6016000	A			H01L-029/00	
EP 1000440	A1	E		H01L-023/48	Based on patent WO 9954934
Designated States (Regional): DE FR GB IT NL					
US 6124198	A			H01L-021/768	Div ex application US 9864431 Div ex patent US 6016000
KR 2001020476	A			H01L-023/48	
JP 2002506577	W		54	H01L-021/768	Based on patent WO 9954934

Abstract (Basic): WO 9954934 A1
Abstract (Basic):
NOVELTY - An ultra-high-speed multilevel **chip** interconnect structure using a free-space dielectric medium is provided for a semiconductor **integrated circuit (IC) chip**.
DETAILED DESCRIPTION - A multilevel interconnect structure for a semiconductor **IC chip** for a semiconductor substrate comprises:
(a) electrically conductive metallization levels with interconnect segments;
(b) plugs for connecting various metallization levels and the semiconductor devices;
(c) a free-space medium occupying at least a portion of the electrically insulating regions within the multilevel interconnect structure; and
(d) an electrically insulating top passivation overlayer for

hermetic sealing and for protection of the **IC chip**, which also serves as a heat transfer medium for facilitating heat removal from the interconnect structure and provides mechanical support for interconnect structure through contact with the top metallization level of the multilevel interconnect structure.

An INDEPENDENT CLAIM is also included for a method for the fabrication of a multilevel interconnect structure.

USE - The method is used for the fabrication of semiconductor **IC chips** to be use in microprocessors and digital signal processors (DSP).

ADVANTAGE - The invention offers improved interconnect structures and methods which will reduce the parasitic effects and enhance the semiconductor **integrated circuit** speed and operational reliability. Simplification at the interconnect process is enabled and **chip** manufacturing cost is reduced. The invention provides the use of a free-space interlevel/intermetal dielectric (ILD/IMD) medium. It is compatible with damascene (single /dual) interconnect fabrication process with a reduced number of process steps per interconnect by four steps. Its compatibility is applicable to various types of interconnect metallization materials such as copper, gold, silver, aluminum, and other superconducting materials. It provides excellent thermal management and efficient heat dissipation removal capabilities. The interconnect structure provides reduce RC propagation delay and reduced capacitive crosstalk. Interconnect metallization electromigration lifetime is improved. It neglects the use of low-k dielectric materials, relatively complex and expensive process integration methods. The invention provides hermetic sealing of the multilevel interconnect structure and semiconductor **IC** devices. It also provides excellent mechanical strength and integrity of the multilevel interconnect structure and overall semiconductor **chip** (claimed).

DESCRIPTION OF DRAWING(S) - The drawing shows a multilevel interconnect structure following formation of an etchant-transmission window pattern on the top layer and after formation of a free-space dielectric medium.

pp; 78 DwgNo 13/15

33/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008526930
WPI Acc No: 1991-031014/199105
XRAM Acc No: C91-013246
XRPX Acc No: N91-024001
Window taper-etching in semiconductor devices mfr. - by initially interposing thin adhesive **layer** between **dielectric** and photoresist **layer**, etc.
Patent Assignee: AMERICAN TELEPHONE & TELEGRAPH CO (AMTT)
Inventor: CHEW H; FIEBER C A; HILLS G W; MARTIN E P
Number of Countries: 006 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 410635	A	19910130	EP 90307848	A	19900718	199105	B
JP 3083064	A	19910409	JP 90196411	A	19900726	199120	
US 5057186	A	19911015	US 90597295	A	19901012	199144	

Priority Applications (No Type Date): US 89387254 A 19890728; US 90597295 A 19901012
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 410635	A				

Designated States (Regional): DE ES FR GB

Abstract (Basic): EP 410635 A

A method is disclosed for etching an opening with a sloping or tapered profile during the mfr. of **integrated circuit** semiconductor devices, where the opening is etched in the presence of a patterned photoresist layer. The etching is effected in the presence of an additional patterned layer chosen to provide adhesion between the photoresist **layer** and the **dielectric**. The etching comprises a first, isotropic etching step and a second, anisotropic etching step, where the material of the additional layer is substantially unaffected during the etching.

ADVANTAGE - The method guards against the sepn. of the photoelectric material from the dielectric during etching.

dwg.4/4

Abstract (Equivalent): US 5057186 A

Prodn. of an **integrated circuit** involves etching a dielectric opening in presence of a patterned photoresist layer, the first etching step being isotropic and the second etching step being anisotropic. Prior to deposition an additional layer is chosen to enhance addn. of photoresist layer.

Pref. dielectric comprises either **SiO2, Si3N4 Si oxynitride**, Al2O3, borosilicate glass, phosphosilicate glass or borophosphosilicate glass.

USE/ADVANTAGE - For making tapered contactor interconnection openings in a dielectric. Enhanced adhesion accurately positions photoresist layer for subsequent anisotropic etching across the remainder of the dielectric thickness by less than 5 microns. (4pp

40/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014725215
WPI Acc No: 2002-545919/200258
XRAM Acc No: C02-154711
XRPX Acc No: N02-432061
Passivation of **integrated circuit** devices for wire bond packaging, involves forming adhesion layer on surface of **insulating layer** by **treating** surface of **insulating layer** with gas
Patent Assignee: INTEL CORP (ITLC)
Inventor: BAKKER G L; DASS M L A; SESHAN K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6352940	B1	20020305	US 98105590	A	19980626	200258	B

Priority Applications (No Type Date): US 98105590 A 19980626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6352940	B1		17	H01L-021/31	

Abstract (Basic): US 6352940 B1
Abstract (Basic):
NOVELTY - An **integrated circuit** (**IC**) device is passivated by forming an **insulating layer** (28) on a substrate (26). An adhesion layer (150) is formed into the surface of the **insulating layer** by **treating** the surface of the **insulating layer** with a gas. A first **passivation layer** is formed on the adhesion **layer**. The first **passivation layer** and the gas include common chemical element(s).
USE - For passivation of **IC** devices used in wire bond packaging.
ADVANTAGE - The inventive method improves adhesion between **insulating layer** and **hard passivation layers** of **integrated circuit** devices to reduce delamination that occurs during the manufacturing process of these devices, such as thermal cycling and sawing.
DESCRIPTION OF DRAWING(S) - The figures show the inventive **integrated circuit** devices.
Substrate (26)
Insulating layer (28)
Adhesion layer (150)
pp; 17 DwgNo 9, 10/21

40/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013788471
WPI Acc No: 2001-272682/200128
XRAM Acc No: C01-082628
XRPX Acc No: N01-194699
Formation of capacitor involves forming selective hemispherical grain silicon layer as second conductive layer after removing **silicon oxynitride** layer through wet etching method utilizing phosphoric acid solution

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: CHIOU J; WANG C

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6204117	B1	20010320	US 99352471	A	19990714	200128	B

Priority Applications (No Type Date): US 99352471 A 19990714
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6204117	B1		11	H01L-021/8242	

Abstract (Basic): US 6204117 B1
Abstract (Basic):

NOVELTY - A capacitor is formed by forming a selective hemispherical grain silicon layer as a second conductive layer over an entire exposed surface of a lower capacitor, after a **silicon oxynitride** layer is removed through a wet etching method utilizing phosphoric acid solution at 150degreesC.

DETAILED DESCRIPTION - Formation of a capacitor includes providing a semiconductor substrate having a semiconductor body. A first **insulating layer** is formed above the substrate and overlies the semiconductor body. The first **insulating layer** is patterned to define a contact hole for the capacitor. An amorphous silicon layer is deposited as a first conductive **layer** over the first **insulating layer** and fills the contact hole. A **silicon oxynitride** layer is formed in the amorphous silicon layer to serve as photo bottom anti-reflective **coating** (BARC) and **hard** mask for capacitor patterns is etched. The **silicon oxynitride** layer and the amorphous silicon layer are patterned to form a lower capacitor electrode. The **silicon oxynitride** layer is removed to expose the entire upper surface of the lower capacitor electrode, through a wet etching method utilizing phosphoric acid (H3PO4) solution at 150degreesC. A selective hemispherical grain (s-HSG) silicon layer as a second conductive layer is formed over the entire exposed surface of the lower capacitor electrode. A second **insulating layer** is formed along a surface of the resulting structure and over the second conductive layer. A third conductive layer is formed over the second **insulating layer** that serves as an upper capacitor electrode.

USE - For forming a capacitor for a dynamic random access memory (DRAM) cell.

ADVANTAGE - The invention enhances the adhesion ability of the **silicon oxynitride** layer into amorphous-**silicon** surface. It provides an increased in space available to imprint

integrated circuits which increases the capacitor area and the cell capacitance. In addition, the size of a chargeable space capable of being stored by the capacitor also increases.

pp; 11 DwgNo 0/2

42/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015368626
WPI Acc No: 2003-429564/200340
XRAM Acc No: C03-113385
XRPX Acc No: N03-342992

Dual damascene process comprises forming first hard mask of metallic materials on low-constant **dielectric layers**, and forming second hard mask on first hard mask

Patent Assignee: HSUE C (HSUE-I); LEE S (LEES-I)
Inventor: HSUE C; LEE S

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030044725	A1	20030306	US 2001910876	A	20010724	200340	B

Priority Applications (No Type Date): US 2001910876 A 20010724
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030044725	A1		23	G03F-007/36	

Abstract (Basic): US 20030044725 A1
Abstract (Basic):

NOVELTY - A dual damascene process comprises:

(i) forming a first hard mask (38) of metallic materials on low-constant (k) **dielectric layers** (361, 362); and

(ii) forming a second hard mask (40) on the first hard mask

DETAILED DESCRIPTION - A dual damascene process comprises:

(a) providing a semiconductor substrate (30) having a conductive structure, **dielectric** separation **layer** (34) covering the conductive structure and a low-k dielectric **layer** over the **dielectric** separation **layer**;

(b) forming a first hard mask of metallic materials on the low-k **dielectric layers**;

(c) forming a second hard mask on the first hard mask;

(d) forming a first opening in the second hard mask over the conductive structure;

(e) forming a second opening in the first hard mask under the first opening, where the diameter of the first opening is larger than the second opening;

(f) removing the low-k **dielectric layer** not covered by the first hard mask until the **dielectric** separation **layer** is exposed to form a via hole;

(g) removing the first hard mask not covered by the second hard mask; and

(h) removing the low-k **dielectric layer** not covered by the first hard mask to reach a predetermined depth so as to form a trench over the via hole.

The trench and the via hole serve as a dual damascene opening.

USE - Used as dual damascene process.

ADVANTAGE - The method prevents oxygen plasma from making contact the low-k **dielectric layer** when a photoresist layer is removed. It increases the gap-filling capacity of the deposited conductive layer in the dual damascene opening. It reduces RC (sic) delay and cross talk, thus allowing **chip** size to be scaled down

to the next generation. It also lowers production cost and simplifies the process.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a dual damascene process.

Substrate (30)

Dielectric separation **layer** (34)

First and second hard masks (38)

Dielectric layers (361, 362)

pp; 23 DwgNo 2L/4

42/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015368250
WPI Acc No: 2003-429188/200340
Related WPI Acc No: 2002-547363
XRAM Acc No: C03-113299
XRPX Acc No: N03-342633
Production of microelectronic device involves depositing layer of photoresist and **layer** of protective **layer** over second **dielectric layer**, and depositing additional layer of photoresist over protective material
Patent Assignee: DANIELS B J (DANI-I); DUNNE J A (DUNN-I); KENNEDY J T (KENN-I)
Inventor: DANIELS B J; DUNNE J A; KENNEDY J T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030032274	A1	20030213	US 2000748692	A	20001226	200340 B
			US 2002243528	A	20020913	

Priority Applications (No Type Date): US 2000748692 A 20001226; US 2002243528 A 20020913
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030032274	A1		39	H01L-021/44	Div ex application US 2000748692

Abstract (Basic): US 20030032274 A1
Abstract (Basic):

NOVELTY - A microelectronic device is produced by sequentially forming a first dielectric **layer**, optional etch stop **layer**, and second **dielectric layer** over a substrate. A layer of photoresist and a layer of protective layer are deposited on top surface of second **dielectric layer**. An addition **layer** of photoresist is deposited on the protective material.

DETAILED DESCRIPTION - Production of microelectronic device comprises sequentially forming a first dielectric **layer**, optional etch stop **layer**, and second **dielectric layer** over a substrate. A layer of photoresist is deposited on top surface of second **dielectric layer** and imagewise removed corresponding to via(s) for the first **dielectric layer**. The portions of each layer under the removed portions of the photoresist are removed to form via(s) down through the first **dielectric layer**. A protective material is deposited on top surface of second **dielectric layer** and on inside wall and a floor of the via. An additional layer of a photoresist is deposited on the protective material. A portion of the photoresist corresponding to the trench for the second **dielectric layer**, is imagewise removed. A portion of each layer under removed portion of additional photoresist layer is removed to form trench or trenches down through the second **dielectric layer**. A barrier metal is lined on inside walls and floor of the trench, and on inside walls and a floor of the via. The trench and via are filled with fill metal in contact with the barrier metal lining.

USE - For producing a microelectronic device useful as

integrated circuit devices.

ADVANTAGE - The process prevents photoresist poisoning. The **dielectric** materials of **insulating layers** are protected by the additional layer from the photoresist material, thus inhibiting the chemical reactions, which cause photoresist poisoning.

DESCRIPTION OF DRAWING(S) - The drawing shows a deep, via first technique together with a deposited protective material.

pp; 39 DwgNo 1b/11

42/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015281757
WPI Acc No: 2003-342689/200332
XRAM Acc No: C03-090046
XRPX Acc No: N03-274090
Dielectric **film** as **coating** and **insulation layer** of device e.g. microfluidic devices, comprises base layer and capping layer
Patent Assignee: CORSO T N (CORS-I); LI J (LIJJ-I); SCHULTZ G A (SCHU-I); ADVION BIOSCIENCES INC (ADVI-N)
Inventor: CORSO T N; LI J; SCHULTZ G A
Number of Countries: 101 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200325992	A1	20030327	WO 2002US29505	A	20020917	200332 B
US 20030057506	A1	20030327	US 2001322862	P	20010917	200336
			US 2002246150	A	20020917	

Priority Applications (No Type Date): US 2001322862 P 20010917; US 2002246150 A 20020917
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200325992	A1	E	33	H01L-021/306	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

US 20030057506	A1		H01L-029/76	Provisional application US 2001322862

Abstract (Basic): WO 200325992 A1
Abstract (Basic):
NOVELTY - A **dielectric film** comprises a base layer and a capping layer. The film is an effective moisture and ion barrier when located between a conductive substrate and a liquid having an electrical potential different than the electrical potential of the substrate.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for preventing the migration of ions from a solution to a conductive substrate having an electrical potential different from that of the solution, comprising providing a **dielectric film layer** comprising a base layer and a **silicon oxynitride** capping layer interposed between the substrate and solution.
USE - For use as a **coating** and **insulation layer** of a device, e.g. microfluidic devices, e.g. electrospray devices and/or liquid chromatography devices, electrophoresis and/or capillary electrochromatography, electrostatic actuation on silicon devices, droplet dispensing devices on conductor using electric fields, or silicon-based fuel injectors.
ADVANTAGE - The **dielectric film** maintains its

electrical properties even when exposed to direct voltage application and high electric field strengths in the presence of high humidity and/or direct liquid contact. It overcomes current **coating** technology limitations and provides appropriate solutions to microfluidic device applications. It allows microfluidic devices to take advantage of high developed silicon processing techniques for silicon and other substrates including micromachining as well as electronic **circuit integration** and electric field definition.

pp; 33 DwgNo 0/3

42/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014690019
WPI Acc No: 2002-510723/200255
XRAM Acc No: C02-145221
XRPX Acc No: N02-404265
Deposition of thin film on substrate for fabricating **integrated circuit**, involves reacting gas mixture of phenyl-based alkoxysilane compound to form organosilicate layer
Patent Assignee: APPLIED MATERIALS INC (MATE-N)
Inventor: GAILLARD F; XIA L; YIEH E
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1209728	A2	20020529	EP 2001124607	A	20011015	200255	B
JP 2002235172	A	20020823	JP 2001361102	A	20011127	200271	
KR 2002041320	A	20020601	KR 200174264	A	20011127	200277	
US 6500773	B1	20021231	US 2000723886	A	20001127	200305	

Priority Applications (No Type Date): US 2000723886 A 20001127
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1209728	A2	E	17	H01L-021/312	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
JP 2002235172	A		16	C23C-016/30	
KR 2002041320	A			H01L-021/20	
US 6500773	B1			H01L-021/31	

Abstract (Basic): EP 1209728 A2
Abstract (Basic):
NOVELTY - A thin film is deposited on a substrate by positioning a substrate (500) in a deposition chamber, providing a gas mixture to the deposition chamber and reacting the gas mixture to form an organosilicate layer (504) on the substrate. The gas mixture comprises a phenyl-based alkoxysilane compound.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(a) a method for forming device comprising forming an organosilicate layer on a substrate and defining a pattern in region(s) of the organosilicate layer;
(b) a method for fabricating a damascene structure comprising forming sequentially a first **dielectric layer** (502) on a substrate and an organosilicate layer, patterning the organosilicate layer to define contacts/vias, forming a second dielectric **layer** on the patterned **layer**, patterning the second **dielectric layer** to define interconnects on the contacts/vias, etching the first **dielectric layer** to form contacts/vias and filling the contacts/vias and the interconnects with a conductive material; and
(c) a computer storage medium containing a software routine that, when executed, causes a general purpose computer to control a deposition chamber according to the above method.
USE - The method is used for depositing thin film useful for **integrated circuit** fabrication, e.g. computer storage

medium containing software.

ADVANTAGE - The organosilicate layer is an anti-reflective **coating** having an absorption coefficient of 0.1-0.7 at a wavelength of less than 250 nm. It has an index of refraction of 1.2-1.7. The absorption coefficient is tunable as a function of the reaction temperature. As the temperature increases the absorption coefficient of the as-deposited layer also increases.

DESCRIPTION OF DRAWING(S) - The figure depicts an schematic cross-sectional views of a damascene structure at different stages of **integrated circuit** fabrication incorporating an organosilicate layer.

Substrate (500)

First **dielectric layer** (502)

Organosilicate layer (504)

pp; 17 DwgNo 5a/5

42/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014635240
WPI Acc No: 2002-455944/200249
XRAM Acc No: C02-129834
XRPX Acc No: N02-359487
Thin film deposition of organosilicate layers, for use in **integrated circuit** production, comprises providing phenyl-based silane compound to deposition chamber, and applying electric field to form organosilicate layer on substrate
Patent Assignee: APPLIED MATERIALS INC (MATE-N)
Inventor: GAILLARD F; LIM T; XIA L; YIEH E
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1180554	A2	20020220	EP 2001118984	A	20010806	200249	B
JP 2002164347	A	20020607	JP 2001245703	A	20010813	200253	
KR 2002013771	A	20020221	KR 200148231	A	20010810	200257	
US 6573196	B1	20030603	US 2000638803	A	20000812	200339	

Priority Applications (No Type Date): US 2000638803 A 20000812
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1180554	A2	E	15	C23C-016/50	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002164347	A		42	H01L-021/316	
KR 2002013771	A			H01L-021/205	
US 6573196	B1			H01L-021/469	

Abstract (Basic): EP 1180554 A2
Abstract (Basic):
NOVELTY - Thin film deposition comprises positioning a substrate in a deposition chamber, supplying a gas mixture to the chamber, which comprises a phenyl-based silane compound, and applying an electric field to the gas mixture in the chamber to form an organosilicate layer on the substrate.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the production of a device comprising forming an organosilicate layer on substrate, in which the layer is formed by applying an electric field to a gas mixture comprising a phenyl-based silane compound, and defining a pattern in at least one region of the layer.
An INDEPENDENT CLAIM is also included for the production of a damascene structure, comprising:
(i) forming a first **dielectric layer** on a substrate;
(ii) forming an organosilicate **layer** on the first **dielectric layer**, in which the organosilicate layer is formed by applying an electric field to a gas mixture comprising a phenyl-based silane compound;
(iii) patterning the organosilicate layer to define contacts/vias through it;
(iv) forming a second **dielectric layer** on the patterned organosilicate layer;
(v) patterning the second **dielectric layer** to define

interconnects through it, in which the interconnects are positioned over the contacts/vias defined in the organosilicate layer;

(vi) etching the first **dielectric layer** to form contacts/vias through it; and

(vii) filling the contacts/vias and the interconnects with a conductive material.

An INDEPENDENT CLAIM is also included for a computer storage medium containing a software routine that, when executed, causes a general purpose computer to control a deposition chamber using a layer deposition method as above.

USE - Used for thin film deposition of organosilicate layers, for use in **integrated circuit** production.

ADVANTAGE - The process allows the deposition of a low dielectric constant material suitable for **integrated circuit** production, in which the low dielectric material is also an anti-reflective **coating** (ARC).

DESCRIPTION OF DRAWING(S) - The figure shows a schematic illustration of an apparatus that can be used for the deposition of a thin film.

Wafer processing system (35)
Process chambers (36, 38, 40, 41)
Load lock chambers (46)
Transfer chambers (50)
Transfer robot (51)
Microprocessor control (54)
pp; 15 DwgNo 1/4

42/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014586697
WPI Acc No: 2002-407401/200244
XRAM Acc No: C02-114520
XRPX Acc No: N02-319967
Formation of layered device such as integrated device, involves introducing gas mixture of silicon and carbon sources and inert gas into deposition chamber, and reacting mixture in presence of preset electric field
Patent Assignee: APPLIED MATERIALS INC (MATE-N)
Inventor: NEMANI S D; XIA L; YIEH E; NEMANI S
Number of Countries: 029 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1191123	A2	20020327	EP 2001307652	A	20010910	200244	B
JP 2002198317	A	20020712	JP 2001277088	A	20010912	200261	
KR 2002022128	A	20020325	KR 200156269	A	20010912	200264	
US 6465366	B1	20021015	US 2000660268	A	20000912	200271	
US 20030008069	A1	20030109	US 2000660268	A	20000912	200311	
			US 2002238195	A	20020909		
US 6589888	B2	20030708	US 2000660268	A	20000912	200353	
			US 2002238195	A	20020909		

Priority Applications (No Type Date): US 2000660268 A 20000912; US 2002238195 A 20020909
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1191123	A2	E	15	C23C-016/32	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002198317	A		46	H01L-021/205	
KR 2002022128	A			H01L-021/205	
US 6465366	B1			H01L-021/31	
US 20030008069	A1			C23C-016/00	Cont of application US 2000660268 Cont of patent US 6465366
US 6589888	B2			H01L-021/31	Cont of application US 2000660268 Cont of patent US 6465366

Abstract (Basic): EP 1191123 A2
Abstract (Basic):
NOVELTY - Formation of a layered device involves positioning a substrate (190) in a deposition chamber (100), introducing a gas mixture comprising a silicon source, a carbon source and an inert gas into the chamber, and reacting the gas mixture in the presence of an electric field to form a silicon carbide layer on the substrate. The electric field is generated using mixed frequency radio frequency (RF) power.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(i) computer program for use in carrying out and controlling operation of forming layered device; and
(ii) computer product which comprises computer program.
USE - For forming a layered device such as an **integrated circuit**.

ADVANTAGE - The silicon carbide layer formed is compatible with **integrated circuit** fabrication processes. The silicon carbide layer is used as a handmask for fabricating **integrated circuit** structures such as damascene structure, and as an anti-reflective **coating** of DUV lithography.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic illustration of an apparatus for forming layered device.

Deposition chamber (100)

Substrate (semiconductor wafer) (190)

pp; 15 DwgNo 1/4

42/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014581455
WPI Acc No: 2002-402159/200243
XRAM Acc No: C02-113174
XRPX Acc No: N02-315305
Formation of damascene interconnect used in manufacturing **integrated circuit** devices involves stripping photoresist layer using sulfur-containing gas that simultaneously forms sidewall **passivation layer**
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: CHOOI S; MEI SHENG Z; XU Y; ZHOU M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6358842	B1	20020319	US 2000633770	A	20000807	200243	B
SG 90781	A1	20020820	SG 20014659	A	20010802	200277	

Priority Applications (No Type Date): US 2000633770 A 20000807
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6358842	B1		14	H01L-021/3205	
SG 90781	A1			H01L-021/3205	

Abstract (Basic): US 6358842 B1
Abstract (Basic):
NOVELTY - Formation of damascene interconnect involves simultaneously stripping away photoresist layer and forming a sidewall **passivation layer** on sidewalls of via openings by using sulfur-containing gas.
DETAILED DESCRIPTION - Formation of damascene interconnect involves providing copper conductor (54) overlying a semiconductor substrate, and a first **passivation layer** (58) overlying the copper conductors. A low **dielectric** constant **layer** (62) is deposited overlying the first **passivation layer**. A photoresist **layer** is deposited overlying the low **dielectric** constant **layer**. The photoresist layer is patterned to form a via mask, and etched through the low **dielectric** constant **layer** to form the via openings. The photoresist layer is stripped away simultaneously forming a sidewall **passivation layer** (82) on the sidewalls of the via openings by using a sulfur-containing gas. The first **passivation layer** is etched to expose underlying copper conductors. A barrier metal layer is deposited overlying the first **passivation layer** and filling the via openings. A copper layer (106) is deposited overlying the barrier metal layer, and filling the via openings. The copper layer is polished down to complete the damascene interconnects in the manufacture of **integrated circuit** device.
USE - For forming damascene interconnect in the manufacture of **integrated circuit** device.
ADVANTAGE - The invention provides a very manufacturable process for forming single or dual damascene interconnects using low dielectric constant materials. By the presence of sidewall **passivation layer**, bowing problem is prevented, anisotropic etching profile is maintained, copper diffusion into the low **dielectric** constant

layers prevented, and via poisoning is avoided.

DESCRIPTION OF DRAWING(S) - The figures show cross-sectional representations of the fabrication of dual damascene interconnect.

Copper conductor (54)
First **passivation layer** (58)
Low **dielectric** constant **layer** (62)
Capping layer (74)
Sidewall **passivation layer** (82)
Second sidewall **passivation layer** (98)
Copper layer (106)
pp; 14 DwgNo 12, 13/13

42/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014581167
WPI Acc No: 2002-401871/200243
XRAM Acc No: C02-113127
XRPX Acc No: N02-315022
Formation of metal interconnect levels in **integrated circuit** by patterning first **dielectric layer** to form trenches for planned damascene interconnects, and depositing conductive barrier **layer** over first **dielectric layer** and lining trenches
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: CHOOI S; GUPTA S; HONG S; ZHOU M S; ZHOU M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6352917	B1	20020305	US 2000598691	A	20000621	200243	B
SG 90775	A1	20020820	SG 20013336	A	20010605	200277	

Priority Applications (No Type Date): US 2000598691 A 20000621
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6352917	B1		44	H01L-021/4763	
SG 90775	A1			H01L-021/4763	

Abstract (Basic): US 6352917 B1
Abstract (Basic):
NOVELTY - Metal interconnect levels are formed by patterning a first **dielectric layer** to form trenches for planned damascene interconnects, depositing conductive barrier **layer** overlying the first **dielectric layer** and lining the trenches, and polishing down a metal layer and the barrier layer to confine them to the trenches and the damascene interconnects.

DETAILED DESCRIPTION - Formation of metal interconnect levels involves depositing a first **dielectric layer** (132) overlying a semiconductor substrate, and comprising stack of dielectric materials. The first **dielectric layer** is patterned to form trenches for planned damascene interconnects. An **insulating layer** is deposited overlying the first **dielectric layer** and lining the trenches. The **insulating layer** is anisotropically etched down the insulating **layer** to form **insulating layer spacers** (409) on the sidewalls of the trenches. The presence of the **insulating layer spacers** prevents metal diffusion into the first **dielectric layer**. A conductive barrier layer (140) is deposited overlying the first **dielectric layer** and lining the trenches. A metal layer (144) is deposited overlying the conductive barrier layer and filling the trenches. The metal layer and the conductive barrier layer are polished down to confine the metal layer and the conductive barrier layer to the trenches and to the damascene interconnects. The damascene interconnects are patterned to form via plugs in an upper portion of the damascene interconnects by partially etching down the damascene interconnects, where a via mask overlies and protects portions of the damascene interconnects from the etching down, where a trench mask overlies and protects the first **dielectric layer** from metal contamination during the etching down, and where portions of the

damascene interconnects partially etched down form conductive lines. A nonconductive barrier layer (164) is deposited overlying the first **dielectric layer**, the conductive lines, and the via plugs. A second **dielectric layer** (168, 172) is deposited overlying the nonconductive barrier layer and filling gaps caused by the patterning of the copper layer to complete the metal interconnect level in the manufacture of the **integrated circuit** device.

USE - For forming metal interconnect levels in the manufacture of an **integrated circuit** device.

ADVANTAGE - The invention provides an effective and very manufacturable method to form metal interconnect levels. It simplifies the barrier layer deposition process and the copper deposition process. It does not require the additional etch stop layer, thus reducing capacitive coupling. Since the via plugs are formed in the same metal layer as the underlying conductive lines, there is no misalignment.

DESCRIPTION OF DRAWING(S) - The figure shows schematically in cross section a metal interconnect.

Etch stopping layer (124)
First **dielectric layer** (132)
Conductive barrier layer (140)
Metal layer (144)
Nonconductive barrier layer (164)
Second **dielectric layer** (168, 172)
Insulating layer spacers (409)
pp; 44 DwgNo 21/42

42/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014511166
WPI Acc No: 2002-331869/200237
XRAM Acc No: C02-095860
XRPX Acc No: N02-260591
Fabrication of **integrated circuit** device involves providing isolation region, forming and removing first gate dielectric **layer**, forming second gate **dielectric layer**, depositing polysilicon **layer**, and patterning these layers
Patent Assignee: CHARTERED SEMICONDUCTOR MFG INC (CHAR-N); CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: FENG G
Number of Countries: 027 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1174919	A2	20020123	EP 2001480056	A	20010717	200237	B
US 6417037	B1	20020709	US 2000618674	A	20000718	200253	

Priority Applications (No Type Date): US 2000618674 A 20000718
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1174919	A2	E	9	H01L-021/8234	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
US 6417037	B1			H01L-021/8238	

Abstract (Basic): EP 1174919 A2
Abstract (Basic):
NOVELTY - **Integrated circuit** device is made by:
(a) providing an isolation region separating two active areas in a semiconductor substrate,
(b) forming a first gate **dielectric layer** overlying the substrate,
(c) removing the first gate **dielectric layer** in the second active area,
(d) forming a second gate **dielectric layer** in the second active area,
(e) depositing a polysilicon layer, and
(f) patterning these layers
DETAILED DESCRIPTION - Fabrication of an **integrated circuit** device involves:
(i) providing an isolation region (12) separating two active areas in a semiconductor substrate (10);
(ii) forming a first gate **dielectric layer** (14) overlying the substrate in the two active areas, where the first gate **dielectric layer** has a first electrical thickness;
(iii) removing the first gate **dielectric layer** in the second active area;
(iv) forming a second gate **dielectric layer** (16) in the second active area, where the second gate **dielectric layer** has a second electrical thickness greater than that of the first and is nitrided;
(v) depositing a polysilicon layer overlying the first and second

gate **dielectric layers**;
(vi) patterning the polysilicon layer and the first and second gate oxide layers to form a first gate transistor (22) in the first active area having the first gate **dielectric layer** under it, and
to form a second gate transistor (24) in the second active area having the second **dielectric layer** under it; and
(vii) completing the **integrated circuit** device.
USE - For the fabrication of **integrated circuit** device.

ADVANTAGE - The method forms both thin and thick gate dielectric thicknesses that can be separately controlled and which are of good quality.
DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional representation of the method.
Substrate (10)
Isolation region (12)
First gate **dielectric layer** (14)
Second gate **dielectric layer** (16)
First gate transistor (22)
Second gate transistor (24)
pp; 9 DwgNo 6/6

42/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014404172
WPI Acc No: 2002-224875/200228
XRAM Acc No: C02-068542
XRPX Acc No: N02-172332
Fabrication of trenches useful in forming copper interconnects involves depositing dissimilar etch stopping **layers** underlying photoresist **layer** and overlying **dielectric** material
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: CHOOI S; LI J; XU Y; ZHOU M S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6331479	B1	20011218	US 99398294	A	19990920	200228	B

Priority Applications (No Type Date): US 99398294 A 19990920
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6331479	B1		13	H01L-021/4763	

Abstract (Basic): US 6331479 B1
Abstract (Basic):
NOVELTY - Trenches are fabricated by depositing a first etch stopping **layer** overlying a first **dielectric layer** and a second etch stopping layer overlying the first etch stopping layer with the first etching stopping layer having a lower etch rate than the second etch stopping layer.
DETAILED DESCRIPTION - Fabrication of trenches involves sequentially depositing on a semiconductor substrate, a first **dielectric layer** (80), a first etch stopping layer (84), a second etch stopping layer (88) and a photoresist layer. The first etch stopping layer has a lower etch rate then the second etch stopping layer. The photoresist layer is patterned to define openings for planned trenches. Etching is performed through the second etch stopping layer to form a hard mask for the planned trenches. The photoresist layer is stripped away by ashing, where the first etch stopping **layer** protects the first **dielectric layer** from damage due to the presence of oxygen radicals. The first etch stopping layer is then etched to complete the trench and the **integrated circuit** is completed.
USE - Fabricating trenches used for forming copper interconnects in the manufacture of **integrated circuit** devices.
ADVANTAGE - Damage to the **dielectric layer** due to oxygen radicals in the ashing plasma is prevented. Poor planarization of **dielectric layers**, trench bowing and via poisoning due to photoresist ashing damage are also prevented.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the fabricated trench.
First **dielectric layer** (80)
First etch stopping layer (84)
Second etch stopping layer (88)
Second **dielectric layer** (100)
First cap layer (104)
pp; 13 DwgNo 14/14

42/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013850367
WPI Acc No: 2001-334580/200135
Related WPI Acc No: 2000-147513; 2002-517685; 2003-491732
XRAM Acc No: C01-103297
XRPX Acc No: N01-241418

New process for forming **dielectric films** or **coatings** on a desired substrate comprises the use of multifunctional surface modification agent

Patent Assignee: ALLIED-SIGNAL INC (ALLC)
Inventor: DRAGE J S; RAMOS T; SMITH D M; VIERNES N; WALLACE S; WU H

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6208014	B1	20010327	US 98111084	A	19980707	200135	B
			US 99235186	A	19990122		

Priority Applications (No Type Date): US 99235186 A 19990122; US 98111084 A 19980707
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6208014	B1		13	H01L-023/58	CIP of application US 98111084

Abstract (Basic): US 6208014 B1
Abstract (Basic):

NOVELTY - Production of a hydrophobic **dielectric film** comprises reacting a suitable hydrophilic silica film with a surface modification agent.

DETAILED DESCRIPTION - Production of hydrophobic **dielectric film** comprises reacting a suitable hydrophilic silica film present on a substrate, with a multifunctional surface modification agent which is a compound of formula selected from R1Si(NR2R3)3, R1Si(ON=CR2R3)3 and/or (R1)xSi(OCOR2)y.

R1 - R3=H, alkyl (preferably 1-18C optionally substituted straight, branched or cyclic alkyl) or aryl (preferably optionally substituted 5-18C aryl);

x=1 or 2; and

y=2 or 3.

An INDEPENDENT CLAIM is also included for an **integrated circuit** comprising at least one **dielectric** silica **film**.

USE - For producing low **dielectric** constant silica **films** on substrates suitable for use in the production of **integrated circuits**.

ADVANTAGE - The improved process provides greater material film strength for a given desired dielectric constant. The surface modification agent significantly reduces the additional appended mass and density added to the film when capping free silanols, relative to the previously employed methods and agents or reagents. The nanoporous films obtained have a moisture stable dielectric constant.

pp; 13 DwgNo 0/2

42/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013788765
WPI Acc No: 2001-272976/200128
XRAM Acc No: C01-082697
XRPX Acc No: N01-194967
Self-aligned dual damascene fabrication for **integrated circuits** (ICs) using a number of etch stop layers and etching processes
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: LIU J; TSAI C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6211063	B1	20010403	US 99318020	A	19990525	200128	B

Priority Applications (No Type Date): US 99318020 A 19990525
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6211063	B1		12	H01L-021/4763	

Abstract (Basic): US 6211063 B1
Abstract (Basic):
NOVELTY - Fabrication comprises:
(1) depositing a 1st etch stop layer on a semiconductor substrate;
(2) depositing a silicate glass layer (35) over the etch stop layer;
(3) depositing a 2nd etch stop layer over the glass layer;
(4) patterning the 2nd etch stop layer to expose the top of silicate glass layer;
(5) depositing a hydrogen silsesquioxane (HSE) layer (46) over the 2nd etch stop layer and exposed silicate glass layer;
(6) depositing an oxide layer (48);
(7) patterning the oxide and hydrogen silsesquioxane layers by reactive ion etching using nitrogen gas to form upper trenches; and
(8) etching away silicate glass layer where not covered by 2nd etch stop layer using reactive ion etching not including nitrogen to form lower trenches.
The lower and overlying upper trenches form dual damascene structures.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the formation of self-aligned dual damascene vias in the fabrication of an **IC** comprising providing 1st metal conductive traces through an **insulating layer** on a semiconductor substrate and carrying out the process above such that the lower trenches overlie the conductive traces and have lateral widths of 0.3-0.5 microns, and the formed upper trenches have lateral widths of 0.4-0.5 microns and overlie the lower trenches. The process further comprises after etching of silicate glass layer, etching of the 1st etch stop layer to reveal the top surfaces of the metal conductive traces and complete the self-aligned dual damascene vias, depositing a 2nd metal layer filling the lower and upper trenches and contacting the conductive traces, and etching back the 2nd metal layer to remove excess metal above the top

surface of the oxide layer to complete the fabrication of the **IC** device.

A further INDEPENDENT CLAIM is included for the formation of self-aligned dual damascene vias in **IC** fabrication using the process above where the etch stop layers are **silicon oxynitride** layers.

USE - Fabrication of self-aligned dual damascene structures in the manufacture of **integrated circuits** (ICs).

ADVANTAGE - The problems of HSQ etch stop and HSQ etch profile bowing are eliminated

DESCRIPTION OF DRAWING(S) - The diagram shows a cross-section of a self-aligned dual damascene via.

Substrate (30)
1st metal layer (32)
Silicon oxide layer (34)
Silicate glass (35)
Fluorinated silicate glass layer (36)
Silicon oxynitride layer (38)
Hydrogen silsesquioxane layer (46)
Plasma enhanced **silicon dioxide** (48)
Passivation layer (56,62)
2nd metal layer (60)
pp; 12 DwgNo 12/12

42/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013653031
WPI Acc No: 2001-137243/200114
XRAM Acc No: C01-040177
XRPX Acc No: N01-099933
Formation of laser accessible fuse for memory arrays by forming fuse with rupture zone, patterning metal layer to form conductive wiring connected to conductive contacts, plate over rupture zone, and wiring pad, patterning **passivation layer**
Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)
Inventor: LIN H; TZENG W; YANG C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6180503	B1	20010130	US 99354852	A	19990729	200114	B

Priority Applications (No Type Date): US 99354852 A 19990729
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6180503	B1		17	H01L-021/44	

Abstract (Basic): US 6180503 B1
Abstract (Basic):
NOVELTY - A laser accessible fuse is formed by forming a fuse with a rupture zone; patterning a metal layer to form conductive wiring connected to at least two conductive contacts, a plate over the rupture zone, and a wiring pad; patterning a **passivation layer** by anisotropically etching the **passivation layer** and an anti-reflective **coating** over a bonding pad, forming a laser access window.
DETAILED DESCRIPTION - A laser accessible fuse is formed by:
(a) depositing a layer of fusible material on a first **insulative layer** on a silicon wafer (70);
(b) patterning the layer of fusible material to form a fuse (78) with a rupture zone (78A);
(c) depositing a second **insulative layer** over the wafer;
(d) forming conductive contacts to the fuse through openings in the second **insulative layer**, where the rupture zone is connected between, and in electrical series with, at least two of the conductive contacts;
(e) depositing a first metal layer (94) on the second **insulative layer**;
(f) patterning the first metal layer to form conductive wiring (96) connected to each of at least two conductive contacts, a plate (86) over the rupture zone, and a wiring pad;
(g) depositing a third **insulative layer** over the wafer;
(h) patterning the third **insulative layer** to form a via opening to the wiring pad, and a window opening over the rupture zone;
(i) depositing a second metal layer (108) on the wafer;
(j) depositing an anti-reflective **coating** (92) on the second metal layer;
(k) patterning a bonding pad in the second metal layer over the via

opening and removing the anti-reflective **coating**, the second metal **layer**, and the first metal layer in the window opening;

(l) depositing a **passivation layer** over the wafer; and

(m) patterning the **passivation layer** by anisotropically etching the **passivation layer** and the anti-reflective **coating** over the bonding pad while simultaneously etching a region within the window opening, penetrating the second **insulative layer** to a final second **insulative layer** thickness over the rupture zone, forming a laser access window.

USE - For forming a laser accessible fuse for memory arrays useful in computer memory **chips**, e.g., dynamic random access memory (DRAM).

ADVANTAGE - The invention (a) allows for a simultaneous etching of the **passivation layer** and bonding pad openings; (b) retards fuse access opening formation during via formation using the transient etch stop layers; (c) improves the uniformity of **insulative layers** over fuse links while at the same time over-etches vias and **passivation layer** access openings to thoroughly remove anti reflection **coating layers**; and (d) uses a single photolithographic mask for patterning a **passivation layer** to form access to bonding pads and laser access openings.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of a DRAM with a fuse access window formed.

Wafer (70)
Fuse (78)
Rupture zone (78A)
Plate (86)
Anti-reflective **coating** (92)
First metal layer (94)
Conductive wiring (96)
Second metal layer (108)
Silicon oxide (118)
Silicon nitride (119)
Polyimide (120)
Passivation layer (122)
pp; 17 DwgNo 2E/2

42/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013595094
WPI Acc No: 2001-079301/200109
XRAM Acc No: C01-022634
XRPX Acc No: N01-060340
Formation of nanoporous **dielectric** silica **coating** on surface of a substrate used in production of **integrated circuits** comprises depositing surface hydrophobizing agent on edge of substrate
Patent Assignee: ALLIED-SIGNAL INC (ALLC)
Inventor: ENDISCH D H; RAMOS T; WU H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6140254	A	20001031	US 98156220	A	19980918	200109	B

Priority Applications (No Type Date): US 98156220 A 19980918
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6140254	A		11	H01L-021/469	

Abstract (Basic): US 6140254 A
Abstract (Basic):

NOVELTY - Formation of a nanoporous **dielectric** silica **coating** on a surface of a substrate (2) comprises spin depositing:

(i) a partially hydrolyzed and condensed fluid alkoxysilane composition (1) onto the substrate surface, and

(ii) a surface hydrophobizing agent on an edge (3) of the substrate surface.

The alkoxysilane composition is cured to a nanoporous **dielectric** silica **coating**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **coated** substrate produced by the above process.

USE - For forming a nanoporous **dielectric** silica **coating** on a surface of a substrate used in the production of **integrated circuits**.

ADVANTAGE - The invention allows the clean removal of an alkoxysilane composition from a substrate edge.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic representation of the cross-sectional side view of the **coated** substrate.

Alkoxysilane composition (1)
Substrate (2)
Edge (3)
pp; 11 DwgNo 6/6

42/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013250034
WPI Acc No: 2000-421917/200036
XRAM Acc No: C00-127516
XRPX Acc No: N00-314781

Polysilicon resistor formation for **integrated circuits**, using oxynitride shield **layer** in interlevel **dielectric** to block diffusion of hydrogen atoms into polysilicon layer

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: CHANG J; CHEN Y; HSU Y; LIN S

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6069063	A	20000530	US 99283841	A	19990401	200036	B

Priority Applications (No Type Date): US 99283841 A 19990401
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6069063	A		11	H01L-021/425	

Abstract (Basic): US 6069063 A
Abstract (Basic):

NOVELTY - A polysilicon resistor is formed having reduced resistance variations by using an oxynitride shield **layer** in the interlevel **dielectric** to block the diffusion of hydrogen atoms into a polysilicon layer.

DETAILED DESCRIPTION - Formation of polysilicon resistor (30) in an **integrated circuit** comprises providing a semiconductor substrate (21) overlaid with a field oxide isolation regions (22), depositing a polysilicon layer over this layer, and etching the polysilicon layer which is not covered by a mask to form a polysilicon resistor. An interlevel **dielectric layer** (40) is then deposited overlying the polysilicon resistor. Nitrogen ions (65) are then implanted into this layer that is then annealed to form a **silicon oxynitride** shield layer (67). Contact openings are then etched through the **dielectric layer** to the polysilicon resistors which is then filled with a metal layer. The metal layer is patterned which is then covered with a **passivation layer** containing hydrogen atoms. The **silicon oxynitride** shield layer prevents hydrogen atoms from penetrating the polysilicon resistor. The **integrated circuit** is then completed.

USE - For forming a polysilicon resistor useful in **integrated circuits**.

ADVANTAGE - Resistivity of the polysilicon resistor is more controlled making resistor values more predictable. The process improves the planarity of the **dielectric interlayer** without increasing the complexity of the process.

DESCRIPTION OF DRAWING(S) - The figure illustrates a cross-sectional representation of the polysilicon resistor.

Semiconductor substrate (21)
Isolation layer (22)
Polysilicon resistor (30)

Interlevel **dielectric layer** (40)
Ion implant (65)
Silicon oxynitride layer (67)
pp; 11 DwgNo 14/15

42/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013084860
WPI Acc No: 2000-256732/200022
XRAM Acc No: C00-078359
XRPX Acc No: N00-190888
Formation of nanoporous **dielectric coating** on a substrate involves depositing a combined composition stream of alkoxysilane composition with base containing catalyst onto a substrate and curing the combined composition
Patent Assignee: ALLIED-SIGNAL INC (ALLC)
Inventor: BRUNGARDT L B; DRAGE J S; RAMOS T; SMITH D M; WU H
Number of Countries: 084 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200013220	A1	20000309	WO 99US18333	A	19990813	200022	B
US 6037275	A	20000314	US 98140855	A	19980827	200022	
AU 9953975	A	20000321	AU 9953975	A	19990813	200031	
EP 1110239	A1	20010627	EP 99939736	A	19990813	200137	
			WO 99US18333	A	19990813		
KR 2001073059	A	20010731	KR 2001702574	A	20010227	200209	
CN 1325541	A	20011205	CN 99812762	A	19990813	200223	
JP 2002524848	W	20020806	WO 99US18333	A	19990813	200266	
			JP 2000568112	A	19990813		
TW 483068	A	20020411	TW 99114035	A	19990817	200313	

Priority Applications (No Type Date): US 98140855 A 19980827
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200013220	A1	E	43	H01L-021/316	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW					
US 6037275	A			H01L-021/316	
AU 9953975	A			H01L-021/316	Based on patent WO 200013220
EP 1110239	A1	E		H01L-021/316	Based on patent WO 200013220
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
KR 2001073059	A			H01L-021/316	
CN 1325541	A			H01L-021/316	
JP 2002524848	W		68	H01L-021/312	Based on patent WO 200013220
TW 483068	A			H01L-021/316	

Abstract (Basic): WO 200013220 A1
Abstract (Basic):
NOVELTY - A nanoporous **dielectric coating** is formed on a substrate by (a) depositing a combined composition stream of alkoxysilane composition with a stream of a base containing catalyst onto a substrate and exposing the combined composition to water or immediately depositing the combined composition onto the substrate; and (b) curing the combined composition.
DETAILED DESCRIPTION - The nanoporous **dielectric**

coating is formed on a substrate by (a) depositing a combined composition stream of alkoxysilane composition with a stream of a base containing catalyst onto a substrate and exposing the combined composition to water or immediately depositing the combined composition onto the substrate; and (b) curing the combined composition. The combined composition stream is unbounded at a point of confluence and the depositing and exposing steps are conducted in order or simultaneously.

An INDEPENDENT CLAIM is also included for a semiconductor device.

USE - The invention is used for producing or forming nanoporous dielectric coatings useful in the production of **integrated circuits**.

ADVANTAGE - The invention forms a nanoporous silica film with more uniform density and film thickness.

pp; 43 DwgNo 0/4

42/3,AB/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013009525
WPI Acc No: 2000-181377/200016
Related WPI Acc No: 1999-363423; 2000-136331; 2001-637979; 2001-662211; 2002-009879
XRAM Acc No: C00-056622
XRPX Acc No: N00-133807
Field effect transistor (FET) for an **integrated circuit** comprising a hafnium or zirconium **silicon oxynitride** dielectric **layer** with substantially higher **dielectric** constant than conventional **silicon** oxide or **nitride**
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: STOLTZ R A; WALLACE R M; WILK G D
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6020243	A	20000201	US 9753616	A	19970724	200016	B
			US 9753617	A	19970724		
			US 98115859	A	19980715		
JP 2000049349	A	20000218	JP 9920082 8	A	19990714	200020	

Priority Applications (No Type Date): US 98115859 A 19980715; US 9753616 P 19970724; US 9753617 P 19970724
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6020243	A		12	H01L-021/283	Provisional application US 9753616
					Provisional application US 9753617
JP 2000049349	A		12	H01L-029/78	

Abstract (Basic): US 6020243 A
Abstract (Basic):
NOVELTY - The **dielectric layer** in the FET comprises hafnium or zirconium **silicon oxynitride** which has a substantially higher dielectric constant than conventional **silicon** oxide or **nitride** and may be made thicker with equivalent field effect, and may be designed to have the advantages of **silicon dioxide**, e.g. high breakdown, low interface state density, and high stability.
DETAILED DESCRIPTION - Fabrication of FET on an **integrated circuit** by; (a) Forming metal **silicon oxynitride** gate dielectric on a single crystal silicon substrate, the metal selected from hafnium, zirconium and their mixtures. (b) Forming a conductive gate over the dielectric.
USE - FETs.
ADVANTAGE - The dielectric has a dielectric constant substantially higher than conventional **silicon** oxide or **nitride** and may be made thicker with equivalent field effect.
DESCRIPTION OF DRAWING(S) - The drawing shows the structure of a FET device
substrate (20)
epitaxial silicon (22)
active channel region (24)
passivation layer (30)
oxynitrided zirconium and silicon layer (42)

42/3,AB/18 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012814631
WPI Acc No: 1999-620862/199953
XRAM Acc No: C99-181336
XRPX Acc No: N99-457918
Deposition of deep submicron metallization within high aspect ratio semiconductor structures for use in the construction of **integrated circuits**
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: LYONS C F; SINGH B
Number of Countries: 021 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9954930	A1	19991028	WO 99US7361	A	19990401	199953	B
EP 1080494	A1	20010307	EP 99916346	A	19990401	200114	
			WO 99US7361	A	19990401		
US 6287959	B1	20010911	US 9865352	A	19980423	200154	
KR 2001042954	A	20010525	KR 2000711779	A	20001023	200168	
JP 2002512449	W	20020423	WO 99US7361	A	19990401	200243	
			JP 2000545191	A	19990401		

Priority Applications (No Type Date): US 9865352 A 19980423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9954930	A1	E	16	H01L-021/768	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1080494	A1	E		H01L-021/768	Based on patent WO 9954930
Designated States (Regional): DE FR GB NL					
US 6287959	B1			H01L-021/4763	
KR 2001042954	A			H01L-021/768	
JP 2002512449	W		19	H01L-021/28	Based on patent WO 9954930

Abstract (Basic): WO 9954930 A1
Abstract (Basic):
NOVELTY - **Silicon oxynitride** films are used both as antireflective coatings and etch stops within deep submicron metallization structures which are commonly patterned using photoresists with deep ultraviolet wavelengths prone to be reflected by metallic surfaces.
DETAILED DESCRIPTION - Depositing metal in deep submicron semiconductor structures comprises depositing a **silicon oxynitride** film over a first metallization layer, conditioning the film to deplete surface nitrogen content, patterning the first metallization layer using deep ultraviolet photolithography, etching the layer, depositing and masking a **dielectric layer**, etching an opening through the **dielectric layer** and stopping etching of the **dielectric layer** upon encountering **silicon oxynitride** film. An INDEPENDENT CLAIM is also included for a deep submicron semiconductor **integrated circuit** interconnect structure comprising a first metallization layer patterned into an interconnect element, a **silicon oxynitride** film deposited over the first metallization layer, the

film being partially etched and functioning as an etch stop, and a second metallization layer deposited over the partially etched film to achieve electrical contact with the first metallization layer.

USE - The method employing **silicon oxynitride films** both as antireflective **coatings** and etch stops is used for multilayer interconnect structures in high density **integrated circuit** manufacturing.

ADVANTAGE - **Silicon oxynitride** can be employed as an antireflective **coating** and an etch stop in patterning deep submicron metallization layers. It has properties compatible with deep ultraviolet photoresists used to pattern highly dense interconnect structures.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a portion of an **integrated circuit** structure.

integrated circuit structure (10)
reflective metal layer (12)
antireflective layer (14)
photoresist (16)
pp; 16 DwgNo 1/5

42/3,AB/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012662519
WPI Acc No: 1999-468624/199939
XRAM Acc No: C99-137376
Nanoporous silica precursor compositions for preparation of dielectric coatings
Patent Assignee: ALLIED-SIGNAL INC (ALLC)
Inventor: DRAGE J; RAMOS T; SMITH D M; WALLACE S
Number of Countries: 082 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9923101	A1	19990514	WO 98US22565	A	19981026	199939	B
AU 9911204	A	19990524	AU 9911204	A	19981026	199940	
EP 1027355	A1	20000816	EP 98953968	A	19981026	200040	
			WO 98US22565	A	19981026		
US 6126733	A	20001003	US 9763815	P	19971031	200050	
			US 98111081	A	19980707		
CN 1285837	A	20010228	CN 98812870	A	19981026	200131	
KR 2001031574	A	20010416	KR 2000704622	A	20000428	200163	
EP 1027355	B1	20020327	EP 98953968	A	19981026	200222	
			WO 98US22565	A	19981026		
DE 69804488	E	20020502	DE 604488	A	19981026	200237	
			EP 98953968	A	19981026		
			WO 98US22565	A	19981026		
TW 504514	A	20021001	TW 98118130	A	19981031	200337	

Priority Applications (No Type Date): US 98111081 A 19980707; US 9763815 P 19971031
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9923101	A1	E	39	C07F-007/04	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 9911204	A				Based on patent WO 9923101
EP 1027355	A1	E		C07F-007/04	Based on patent WO 9923101
Designated States (Regional): DE FR GB IE NL					
US 6126733	A			C09D-103/00	Provisional application US 9763815
CN 1285837	A			C07F-007/04	
KR 2001031574	A			C07F-007/04	
EP 1027355	B1	E		C07F-007/04	Based on patent WO 9923101
Designated States (Regional): DE FR GB IE NL					
DE 69804488	E			C07F-007/04	Based on patent EP 1027355
					Based on patent WO 9923101
TW 504514	A			C07F-007/04	

Abstract (Basic): WO 9923101 A1
Abstract (Basic):
NOVELTY - Nanoporous silica precursor compositions containing one or more alkoxysilane, a low volatility solvent comprising at least 1 1-4C alkyl ether of a 1-4C alkylene glycol and at least 1 high

volatility solvent composition having a boiling point below that of the low volatility solvent composition.

DETAILED DESCRIPTION - Nanoporous silica precursor compositions containing:

(a) one or more alkoxysilane;

(b) a low volatility solvent comprising at least 1 1-4C alkyl ether of a 1-4C alkylene glycol which:

(i) is miscible in water and alkoxysilanes;

(ii) has a hydroxyl concentration of at most 0.0084 mole/cm3;

(iii) has a boiling point of at least 175 degreesC (atmospheric pressure); and

(iv) has an average molecular weight of at least 120;

(c) at least 1 high volatility solvent composition having a boiling point below that of the low volatility solvent composition;

(d) optionally water; and

(e) optionally an acid catalyst.

INDEPENDENT CLAIMS are included for

(1) a method of forming a nanoporous **dielectric coating** on a substrate, by:

(a) blending the above nanoporous silica precursor composition to form a mixture to cause a partial hydrolysis and partial condensation of the alkoxysilane;

(b) depositing the composition onto a substrate while evaporating at least part of the relatively high volatility solvent composition;

(c) exposing the composition to a water vapor and a base vapor; and

(d) evaporating the relatively low volatility solvent composition to form a relatively high porosity, low dielectric constant, silicon containing polymer composition on the substrate.

(2) The **coated** substrate formed by the above process; and

(3) A semiconductor device produced by the above process in which the substrate is a semiconductor substrate.

USE - The process is useful for forming the nanoporous **dielectric coating** on a substrate, e.g. crystalline silicon, polysilicon, amorphous silicon, epitaxial **silicon**, and **silicon dioxide**. The substrate also comprises a raised pattern of lines of a metal, an oxide, a nitride and/or an oxynitride material or a semiconductor material, preferably silicon or gallium arsenide and silica, **silicon nitride**, titanium **nitride**, tantalum nitride, aluminum or alloys, copper or alloys, tantalum, tungsten and/or **silicon oxynitride**, which are used to form conductors and insulators. The method can be used in making semiconductor devices especially microelectronic **integrated circuits**.

ADVANTAGE - The method provides a precursor solution which is stable over periods of months, from which can be obtained films of high quality having, e.g. high surface area, high mechanical strength, small pore size and no defects or large pores. The use of ultrapurified materials reduces the amount of trace metals in the resulting nanoporous layer and results in a reduction of layer interference, e.g. RC delay, power consumption and crosstalk in the final product **integrated circuit**.

pp; 39 DwgNo 4/4

42/3,AB/20 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012598540
WPI Acc No: 1999-404646/199934
XRAM Acc No: C99-119359
XRPX Acc No: N99-301614
Psi shaped electrode used in capacitor for dynamic random access memory
Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)
Inventor: CHEN L Y; LIAW I
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5923973	A	19990713	US 97957674	A	19971024	199934	B

Priority Applications (No Type Date): US 97957674 A 19971024
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5923973	A		13	H01L-021/8242	

Abstract (Basic): US 5923973 A
Abstract (Basic):
NOVELTY - The capacitor is formed by depositing **dielectric layers** over an area of a semiconductor incorporating active devices, patterning the top **dielectric layer** to form a capacitor hole, plating the sides and bottom of the hole with a conductive layer, etching a contact hole though the bottom of the capacitor hole and filling with a conductive material and removing the remaining dielectric to leave a capacitor electrode with a Greek psi shape. This is then covered with an **insulating film** and then a second conductor to form a capacitor.

DETAILED DESCRIPTION - The capacitor is fabricated by:

(a) Depositing and planarising a first **dielectric layer** (30) onto a semiconductor substrate (10) incorporating active devices.

(b) Depositing a second **dielectric layer** (32).

(c) Depositing a third **dielectric layer**.

(d) Patterning this third layer to form capacitor holes by etching the third layer away to reveal the top surface of the second **dielectric layer**.

(e) Depositing a layer of conductive material (36) on the sides and bottom of the capacitor hole.

(f) Filling the hole with a fourth dielectric.

(g) Forming a contact hole down through the fourth dielectric that extends on down through the conductive layer (36) and the second (32) and first (30) **dielectric layers** to expose the underlying contact regions (14) in the active circuit area.

(h) Filling the hole with a second conductive material (41).

(i) Etching away the top most parts of the first and second conductive films that are on top of the third **dielectric film**.

(j) Etching away the remaining parts of the third and the fourth **dielectric films** to leave a psi shaped capacitor electrode (36,41).

(k) Depositing a fifth conformal **dielectric layer** (48) on the electrode structure.

(l) Depositing a third conductive layer (50) on top of the

conformal layer to form the second capacitor electrode.

(m) Patterning the third conductive and fifth **dielectric layers** to form capacitors.

USE - Forming capacitors in semiconductor devices, particularly dynamic random access memories (DRAM's).

ADVANTAGE - The capacitors have a large surface area and hence a large capacitance while occupying a small surface area on the **chip**.

DESCRIPTION OF DRAWING(S) - The drawing shows a completed capacitor.

Substrate (10)
First **dielectric layer** (30)
Second **dielectric layer** (32)
First conductive layer (36)
Contact region (14)
Contact plug (41)
Fifth **dielectric layer** (48)
Third conductive layer (50)
Hemispherical polysilicon (44)
pp; 13 DwgNo 20/20

42/3,AB/21 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012495999
WPI Acc No: 1999-302107/199925
Related WPI Acc No: 2001-089914
XRAM Acc No: C99-088545
XRPX Acc No: N99-226331
Interconnect structure for ultra-large scale intergrated circuits has sections of **dielectric interlayers** not supporting conductive patterns removed to form air gaps that are filled with low dielectric constant materials
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: WOLLESEN D L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5900668	A	19990504	US 95564998	A	19951130	199925	B

Priority Applications (No Type Date): US 95564998 A 19951130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5900668	A		11	H01L-029/00	

Abstract (Basic): US 5900668 A
Abstract (Basic):

NOVELTY - Sections of **dielectric interlayers** not supporting conductive patterns are removed by anisotropic etching to form air gaps (20) which can be removed or filled with a low dielectric constant material.

DETAILED DESCRIPTION - Semiconductor device has sequential **dielectric** and conductive **layers**. Each conductive layer is patterned, and each **dielectric layer** has a part of a first dielectric material underneath the conductive pattern, and a part of a second dielectric material with a lower dielectric constant between them. The first material is **silicon dioxide**, and the second is polyimide or other organic dielectric.

USE - Forming interconnect structures for ultra-large scale **integrated circuits**.

ADVANTAGE - Parasitic capacitance is reduced, allowing increased **integrated circuit** speed.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the device, with sections of the **dielectric layers**.

source (2,2')
drain (3,3')
field oxide region (4)
gate electrodes (6)
gate oxide (7)
first **dielectric layer** (8)
contacts (9)
first conductive layer (10)
second **dielectric layer** (11)
vias/plugs (12,15)
second conductive layer (13)
third **dielectric layer** (14)
third conductive layer (16)
air spaces (20)

42/3,AB/22 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008262441
WPI Acc No: 1990-149442/199020
Related WPI Acc No: 1990-276482; 1991-111272; 1991-119176; 1991-240187
XRAM Acc No: C90-065406
XRPX Acc No: N90-115836
Low-melting inorganic glass planarising of **IC** - eliminates separate **coating**, drying and curing steps and minimises contamination
Patent Assignee: APPL MATERIALS INC (MATE-N); APPLIED MATERIALS INC (MATE-N)
Inventor: LAW K S; MARKS J; MAYDAN D; WANG D N K; MAYDEN D; WANG D N
Number of Countries: 013 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 368504	A	19900516	EP 89310921	A	19891024	199020 B
JP 2199831	A	19900808	JP 89289850	A	19891107	199038
US 5112776	A	19920512	US 88269508	A	19881110	199222
			US 90541449	A	19900621	
			US 91644853	A	19910122	
US 5244841	A	19930914	US 88269508	A	19881110	199338
			US 90541449	A	19900621	
			US 91644853	A	19910122	
			US 91805423	A	19911210	

Priority Applications (No Type Date): US 88269508 A 19881110; US 90541449 A 19900621; US 91644853 A 19910122; US 91805423 A 19911210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 368504	A				
Designated States (Regional): AT BE CH DE ES FR GB IT LI NL SE					
US 5112776	A		11	H01L-021/461	Cont of application US 88269508
					Cont of application US 90541449
US 5244841	A		10	H01L-021/465	Cont of application US 88269508
					Cont of application US 90541449
					Cont of application US 91644853
					Cont of patent US 5112776

Abstract (Basic): EP 368504 A

A method of planarising an **IC** (10) using a low-melting inorganic glass comprises depositing an **insulating layer** (20) over an **IC** structure, depositing the low-melting inorganic planarising layer (30) over this and etching it to planarise the structure. Also claimed is a process as above in which the **insulating layer** is **Si** oxide, **nitride**, or **oxynitride**, the low-melting glass is B2O3, B2S6, or B2O3/**SiO2** mixts., As2O3, As2S3, or P2O5, or a combination of these, having a m.pt. below 575 deg.C and a flow temp. of 500 deg.C or less, and planarisation is by anisotropic dry etching.

Further claimed is a process as above in which the **insulating layer** is Si oxide, the glass is P2O5 having a m.pt. of 480 deg.C and a flow temp. of 390 deg.C or less, and anisotropic dry etching removes all of the planarising material and part of the **insulating layer** to planarise the structure.

Additionally claimed is a process as above comprising depositing an Si oxide insulator over an **IC** having closely spaced raised portions, removing part of the insulation between these portions, depositing a second, similar, **insulating layer** over the first, depositing the inorganic planarising layer, and anisotropically etching to planarise.

USE/ADVANTAGE - A method of planarising **IC** structures which avoids the use of intermediate deposition or **coating**, solvent evapn. or baking steps outside the vacuum appts. is provided. The risk of contamination is much reduced and expensive and time-consuming steps eliminated. (11pp Dwg.No.2/9)

Abstract (Equivalent): US 5112776 A

Process comprises: (a) depositing a 1st **layer** of **insulating** material over an **IC** structure in a CVD zone; (b) depositing a low m.pt. inorganic planarising layer having a flow temp. not above 500 deg.C in the CVD zone at 300-500 deg.C and high enough to permit flow as it is deposited; and (c) dry etching the planarising layer in an etching zone until all of the layer has been removed. The planarising layer is B203, B2S6, B203/Si02 mixts. As203, As2S3, P205 or their mixts.. The **insulating layer** is oxide, **nitride** or **oxynitride** of **Si**. ADVANTAGE - No intermediate deposition, **coating**, solvent evapn. or baking is needed, and the same appts. may be used to deposit the **insulating** and planarising **layers**.

42/3,AB/23 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007617952
WPI Acc No: 1988-251884/198836
XRPX Acc No: N88-191577
IC structure formation system preventing void formation - controls compressive stress in **silicon nitride** layer for moisture and ion penetration
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: ALLEN B L; BOWERS T R; GWOZDZ P S
Number of Countries: 015 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 281324	A	19880907	EP 88301637	A	19880225	198836	B
JP 63228627	A	19880922	JP 8850574	A	19880302	198844	
US 5010024	A	19910423	US 89353169	A	19890515	199120	
EP 281324	B1	20000719	EP 88301637	A	19880225	200037	
DE 3856418	G	20000824	DE 3856418	A	19880225	200043	
			EP 88301637	A	19880225		

Priority Applications (No Type Date): US 8721828 A 19870304; US 89353169 A 19890515
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 281324	A	E	10		
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
EP 281324	B1	E		H01L-021/318	
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
DE 3856418	G			H01L-021/318	Based on patent EP 281324

Abstract (Basic): EP 281324 A

The **integrated circuit** has a metal layer underlying a **silicon nitride** encapsulating layer for the prevention of moisture and ion contamination penetration. The metal layer is stress relieved to prevent the formation of voids resulting from the compressive stress in the encapsulating layer. The metal layer may be stress relieved by ion implantation to change its surface grain structure.

The compressive stress in the encapsulating **silicon nitride** is reduced by choice of reactor pressure during layer formation. Stress relief is aided by formation of an intermediate layer between the metal and encapsulating layers.

USE/ADVANTAGE - Particularly for EEPROMS. Permits use of ultra-violet transparent **silicon nitride passivating layer** while avoiding breaks in underlying metal wiring.

0/1

Abstract (Equivalent): US 5010024 A

The method comprises stress relieving the underlying metal layer from stresses induced by the compressive stress of a **silicon nitride** encapsulating layer to inhibit the formation of voids therein by implanting the metal layer with ions to change the grain structure adjacent the surface of the metal **layer**. An **insulating** intermediate **layer** is formed between the layer and the **silicon nitride** layer selected from the class consisting of an oxide of **silicon** and **silicon**

oxynitride having a compressive/tensile stress which sufficiently compensates for the compressive stess of the **silicon nitride** layer.

The compressive stress is controlled in the **silicon nitride** layer to provide resistance to moisture and ion penetration superior to **silicon dioxide** or **silicon oxynitride** layers of similar thickness while inhibiting formation of voids in the metal layer.

ADVANTAGE - Excellent resistance to penetration by moisture and ion contaminants and a substantial absence of voids in an underlying metal layer in the structure, and, in the case of EPROMS, maintaining sufficient UV light transmissity to permit erasure

42/3,AB/24 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002554645
WPI Acc No: 1980-72668C/198041
Semiconductor mfr. with improved **insulating film** - by depositing **silicon dioxide** film on **silicon** substrate, then heating surface in gas plasma atmos. contg. nitrogen
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 55113335	A	19800901				198041 B

Priority Applications (No Type Date): JP 7920331 A 19790223

Abstract (Basic): JP 55113335 A

A semiconductor device is made by depositing a **silicon dioxide** film on a **silicon** substrate, and then heat treating the surface of the **silicon dioxide** film in a gas plasma atmosphere contg. nitrogen to substitute nitrogen for oxygen as a constituent of the **silicon dioxide** film at least in one part of the film.

A dense and stable **insulating film** having improved impurity contamination preventing property is thus formed on the surface of a semiconductor substrate. A **SiO2** film has been used as a **passivatin film** on a silicon device, however, the surface of the **SiO2** film is often contaminated with impurities. Such a disadvantage is eliminated by forming the oxynitride film at least on the surface of the **silicon** dioxide film. The **silicon oxynitride** film made from the **silicon dioxide film** by heat **treatment** in N2 has dense and defect-free structure. The film is pref. used in an MOS **IC**.

(FILE 'HOME' ENTERED AT 11:48:50 ON 25 AUG 2003)

FILE 'REGISTRY' ENTERED AT 11:50:19 ON 25 AUG 2003

```
L1            48 S O2 SI/MF
L2           366 S N.O.SI/MF OR N O SI/ELF
L3           803 S N.SI/MF OR N SI/ELF
                 E N4.SI3/MF
```

FILE 'CAPLUS' ENTERED AT 12:00:26 ON 25 AUG 2003

```
L4        509781 S L1 OR (SILICON OXIDE) OR SILICA
L5          4756 S L2 OR (SILICON OXYNITRIDE)
L6         71637 S L3 OR (SILICON NITRIDE)
L7         15652 S L4 AND ((INTEGRAT########(3N)(CIRCUIT######## OR LOOP)) OR IC
L8          4079 S L7 AND ((INSULAT######## OR DIELECTR########)(3N)(LAYER### OR
L9           147 S L8 AND ((ADHESIVE OR ADHERE### OR ATTACH####### OR SECUR#####
L10           25 S L9 AND ((PASSIVAT######## OR COAT###### OR TREAT######)(3N)(L
L11           25 DUP REM L10 (0 DUPLICATES REMOVED)
L12          122 S L9 NOT L10
L13            0 S L12 AND ((PHOTODEFIN######## OR PHOTO()DEFIN########)(3N)(PAS
L14            0 S L12 AND ((SOFT OR HARD)(3N)(PASSIVAT######## OR COAT###### OR
L15            0 S L12 AND (OXYD########(3N)(LAYER### OR FILM### OR COAT### OR M
L16        27805 S L4 AND ((INSULAT######## OR DIELECTR########)(3N)(LAYER### OR
L17           68 S L5 AND ((ADHESIVE OR ADHERE### OR ATTACH####### OR SECUR#####
L18         5632 S L6 AND ((PASSIVAT######## OR COAT###### OR TREAT######)(3N)(L
L19         1033 S L16 AND L18
L20            3 S L19 AND L17
L21            3 DUP REM L20 (0 DUPLICATES REMOVED)
```

L11 ANSWER 1 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:23379 CAPLUS
DN 138:81917
TI ULSI wiring and method of manufacturing the same
IN Ueno, Kazuyoshi; Osaka, Tetsuya; Takano, Nao
PA Waseda University, Japan; NEC Corporation
SO U.S. Pat. Appl. Publ., 12 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003008075	A1	20030109	US 2002-154812	20020528
	JP 2003051538	A2	20030221	JP 2001-277602	20010913
	US 2003124263	A1	20030703	US 2002-315078	20021210
	US 2003124255	A1	20030703	US 2002-315099	20021210
PRAI	JP 2001-158513	A	20010528		
	JP 2001-277602	A	20010913		
	US 2002-154812	A3	20020528		

AB A method of manufg. ULSI wiring in which wiring layers are sep. formed via a diffusion prevention **layer** with an **insulating interlayer** portion made of SiO2. The method comprises the steps of treating, with a silane compd., an SiO2 surface on which the **insulating interlayer** portion is to be formed, performing catalyzation with an aq. soln. contg. a Pd compd., forming the diffusion prevention layer by electroless plating, and then forming the wiring layer on this diffusion prevention layer. Also, a capping layer is formed on the wiring layer by electroless plating. In consequence, the diffusion prevention **layer** having good **adhesive** properties can all be formed through a simple process by wet processes, and further, the wiring layer can directly be formed on this diffusion prevention layer by the wet process. The capping layer can directly be formed on this wiring layer by the electroless plating.

L11 ANSWER 2 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:312638 CAPLUS
DN 138:296090
TI Method for forming copper pad redistribution on a semiconductor substrate
IN Lee, Tze Liang
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6551856	B1	20030422	US 2000-637223	20000811
PRAI	US 2000-637223		20000811		

AB The present invention generally relates to a method for forming input/output pad redistribution on a semiconductor substrate and device formed and more particularly, relates to a method for forming copper pad redistribution in a flip **chip** that is compatible with copper dual damascene process and a flip **chip** package formed. The method is compatible with a Cu dual damascene process such that, after a substrate surface is planarized by chem. mech. polishing, a single

photomask can be used to pattern a plurality of redistribution pads, redistribution vias and redistribution lines. After the openings are filled with Cu by an electroplating or an electroless plating technique, the top of the structure is again chem. mech. polished to produce a planarized surface and resulting redistribution pads and redistribution lines. A **sealing layer** such as Si nitride may be coated on the final structure as a moisture barrier.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 3 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:75599 CAPLUS
DN 138:129833
TI Semiconductor devices having a **passivation film** in **chip**-molded semiconductor packages
IN Yamashita, Atsuko; Kobayashi, Motoomi; Takimoto, Kazuhiro
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2003031655	A2	20030131	JP 2001-210977	20010711
PRAI	JP 2001-210977		20010711		

AB The title devices comprise (1) an electrode circuit formed on a semiconductor substrate, (2) a 1st **insulator film** which has a thermal expansion coeff. smaller than that of the electrode circuit and coats over the electrode circuit on the substrate, (3) a 2nd **insulator film** which has a thermal expansion coeff. greater than that of the 1st **insulator film** and is formed around the substrate periphery and seals the sidewalls of the electrode circuit, (4) a 3rd **insulator film** which has a thermal expansion coeff. greater than that of the 2nd **insulator film** and **coats** over the 2nd and 1st **insulator films**, and (5) a molding polymer which has a thermal expansion coeff. greater than that of the 3rd **insulator film** and **seals** around the substrate. The 1st, 2nd, and 3rd **insulator films** are made of an inorg. material, SOG, and polyimide, resp. The electrode circuit may be made of Al provided on the top circuit layer in the multilayer circuit boards. The arrangement of the **insulator films** gives the devices prevention of circuit wire sliding and **passivation film** cracking in **chip** packaging.

L11 ANSWER 4 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:616120 CAPLUS
DN 137:178102
TI **Chip** structure with improved resistance-capacitance delay and process for forming the same
IN Lin, Mou-shiung; Lee, Jin-yuan; Huang, Ching-cheng
PA Taiwan
SO U.S. Pat. Appl. Publ., 30 pp., Cont.-in-part of U. S. Ser. No. 216,791, abandoned.
CODEN: USXXCO
DT Patent
LA English

FAN.CNT 6

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002109232	A1	20020815	US 2002-124388	20020415
	US 6383916	B1	20020507	US 1999-251183	19990217
	US 6495442	B1	20021217	US 2000-691497	20001018
	US 2002048930	A1	20020425	US 2001-972639	20011009
	US 2003071326	A1	20030417	US 2002-303451	20021125
	US 2003107136	A1	20030612	US 2003-337673	20030106
PRAI	US 1998-216791	B2	19981221		
	US 1999-251183	A2	19990217		
	US 2000-691497	A2	20001018		
	US 2001-972639	A2	20011009		
	US 2001-970005	A1	20011003		
	TW 2001-90130876	A	20011213		
	TW 2001-90131030	A	20011214		
	TW 2001-90131796	A	20011221		
	US 2002-124388	A3	20020415		

AB The invention relates in general to a **chip** structure and a process for forming the same. More particularly, the invention relates to a **chip** structure for improving the resistance-capacitance delay and a forming process thereof. A **chip** structure comprises a substrate, a 1st built-up **layer**, a **passivation layer** and a 2nd built-up layer. The substrate includes many elec. devices placed on a surface of the substrate. The 1st built-up layer is located on the substrate. The 1st built-up layer is provided with a 1st dielec. body and a 1st interconnection scheme, in which the 1st interconnection scheme interlaces inside the 1st dielec. body and is elec. connected to the elec. devices. The 1st interconnection scheme is constructed from 1st metal layers and plugs, in which the neighboring 1st metal **layers** are elec. **connected** through the plugs. The **passivation layer** is disposed on the 1st built-up layer and is provided with openings exposing the 1st interconnection scheme. The 2nd built-up layer is formed on the **passivation layer**. The 2nd built-up layer is provided with a 2nd dielec. body and a 2nd interconnection scheme, in which the 2nd interconnection scheme interlaces inside the 2nd dielec. body and is elec. connected to the 1st interconnection scheme. The 2nd interconnection scheme is constructed from at least one 2nd metal layer and at least one via metal filler, in which the 2nd metal **layer** is elec. **connected** to the via metal filler. The thickness, width, and cross-sectional area of the traces of the 2nd metal layer are resp. larger than those of the 1st metal layers.

L11 ANSWER 5 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:221078 CAPLUS
DN 136:255745
TI Method for forming a bump, semiconductor device and method of fabricating same, semiconductor **chip**, circuit board, and electronic instrument
IN Matsushima, Fumiaki; Ota, Tsutomu; Makabe, Akira
PA Japan
SO U.S. Pat. Appl. Publ., 24 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	US 2002033531	A1	20020321	US 2001-945241	20010831
	CN 1359147	A	20020717	CN 2001-141243	20010904
PRAI	JP 2000-267076	A	20000904		

AB A method for forming a bump includes the steps of forming a resist layer so that a through-hole formed therein is located on a pad; and forming a metal **layer** to be elec. **connected** to the pad conforming to the shape of the through-hole. The metal layer is formed so as to have a shape in which is formed a region for receiving a soldering or brazing material.

L11 ANSWER 6 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:461278 CAPLUS
DN 137:26945
TI Soft plasma oxidizing plasma method for forming carbon doped silicon containing **dielectric layer** with enhanced **adhesive** properties
IN Li, Lain-jong; Bao, Tien-i; Lin, Cheng-chung; Jang, Syun-ming
PA Taiwan Semiconductor Manufacturing Co., Ltd, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6407013	B1	20020618	US 2001-761422	20010116
PRAI US 2001-761422		20010116		

AB The invention relates to a process for making a semiconductor **integrated circuit** device. Within a method for forming a **dielec. layer** within a microelectronic fabrication there is first provided a substrate. There is then formed over the substrate a carbon doped silicon contg. **dielec. layer**. There is then treated the carbon doped silicon contg. **dielec. layer** with an oxidizing plasma to form from the carbon doped silicon contg. **dielec. layer** an oxidizing plasma **treated** carbon doped silicon contg. **dielec. layer**. By treating the carbon doped silicon contg. **dielec** . **layer** with the oxidizing plasma, particularly under mild conditions, to form therefrom the oxidizing plasma treated carbon doped silicon contg. **dielec. layer**, adhesion of an addnl. microelectronic layer upon the oxidizing plasma treated carbon doped silicon contg. **dielec. layer** is enhanced in comparison with adhesion of the addnl. microelectronic layer upon the carbon doped silicon contg. **dielec. layer**, while not compromising **dielec.** properties of the carbon doped silicon contg. **dielec. layer**.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 7 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:833769 CAPLUS
DN 135:365336
TI Semiconductor **integrated circuit** with an insulation structure having reduced permittivity
IN Lien, Chuen-der; Lee, S. K.
PA USA
SO U.S. Pat. Appl. Publ., 11 pp., Cont. of U.S. Ser. No. 775,345.

CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2001040267	A1	20011115	US 2001-791316	20010223
US 6576976	B2	20030610		
PRAI US 1997-775345	A1	19970103		

AB A 1st **insulating layer** overlying semiconductor substrate has a plurality of conductive paths disposed thereon. Each of the plurality of conductive paths has at least a major portion thereof overlied with a 2nd **insulating layer**. A 3rd **insulating layer**, having air gap ports formed therein, overlies adjacent conductive paths and extends from one to another such that an air gap is formed. A **passivation layer** overlies 3rd **insulating layer** and **seals** the plurality of air gaps ports to form an insulation structure for a semiconductor **integrated circuit**, and method thereof.

L11 ANSWER 8 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:181192 CAPLUS
DN 134:216002
TI Photoelectric devices
IN Tsuda, Hiroyuki; Nakahara, Tatsushi; Ishihara, Noboru; Terui, Hiroshi; Ishibashi, Tadao
PA Nippon Telegraph and Telephone Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001068720	A2	20010316	JP 1999-238795	19990825
PRAI JP 1999-238795		19990825		

AB The title devices comprise a protective **layer-coated** electronic **circuit** substrate and an **integrated** photoelec. transducer components formed over an **insulator layer** on the substrate. The protective layer has (1) a 1st contact hole connecting the 1st electrode in the photoelec. transducer and the electronic circuit and (2) a 2nd contact hole connecting the 2nd electrode in the photoelec. transducer and the circuit.

L11 ANSWER 9 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:117655 CAPLUS
DN 134:186963
TI Multilayer printed circuit boards and fabrication thereof
IN Fushie, Takashi; Kagatsume, Takeshi; Matsui, Shigekazu
PA Hoya Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 19 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001044639	A2	20010216	JP 2000-149570	20000522

	JP 2003204152	A2	20030718	JP 2002-377945	20000522
	US 6339197	B1	20020115	US 2000-579270	20000526
	TW 479335	B	20020311	TW 2000-89110253	20000526
	US 2002100608	A1	20020801	US 2001-3103	20011206
PRAI	JP 1999-147811	A	19990527		
	JP 2000-149570	A3	20000522		
	US 2000-579270	A3	20000526		

AB The title fabrication involves (1) opening through holes by photolithog. to a photochem. glass which has a thermal expansion coeff. similar to the Cu film layer., (2) sputtering a **silica** layer and Si nitride layer for prevention of metal ion leakage from the photochem. glass, (3) sputtering a Cr layer, a Cr-Cu layer, and a Cu layer for increasing adhesion between the Cu film layer and the sputtered **silica** layer, (4) depositing a Cu film with its thickness 1-20 .mu.m, (5) filling the through holes with a polymer, (6) etching to pattern the circuit **layer**, (7) forming an **insulator layer**, and (7) subsequently **treating** and **coating** the surface with a cover **coating layer**. The process gives the circuit boards fine and precision integration with smaller sized through holes.

L11 ANSWER 10 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:50417 CAPLUS
DN 134:124545
TI Multilayer printed circuit boards and fabrication thereof
IN Murai, Toshikinu; Kawamoto, Kenji
PA Toppan Printing Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001015934	A2	20010119	JP 1999-185873	19990630
PRAI	JP 1999-185873		19990630		

AB The title circuit boards are prepd. by alternately laminating with an electroless plated/electrolytic plated conductor pattern and a thermal resistant polymer **insulator layer**, optionally contg. **silica** microparticles. The polymer **insulator layers** are **coated** with **adhesive layer** contg. a polyfunctional epoxy compd., a hardening agent, epoxy silane coupling agent, and an alkoxysilane. The use of the **adhesive layer** gives the conductor pattern increased adhesion strength and reliable highly **integrated** multilayer printed **circuit** boards.

L11 ANSWER 11 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:701910 CAPLUS
DN 133:275195
TI Thin **film** electronics on **insulator** on metal
IN Harris, Ellis D.
PA USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	US 6127725	A	20001003	US 1998-128107	19980803
PRAI	US 1998-128107		19980803		

AB An electronics module consists, generally of a refractory metal sheet, **coated** with a refractory **insulator film**, which in turn is **coated** with a **film** of Si within, which thin film transistor electronics circuits are further generated along with interconnection means. Particulate matter is deposited in a desired pattern by a printing process and then fused into smooth thin films by means of an IR laser. Insulator particles are 1st deposited onto the refractory metal sheet and then melted and fused into a smooth **film adhered** to the metal sheet. Si particles are next deposited on the **insulator film** and melted and crystd. into electronic quality Si film. TFT electronics are next generated in the Si by known means. A plurality of individual modules can be disposed in patches over an extended area both conserving material and providing mech. flexibility as required by certain applications. Addnl., a plurality of individual modules can be arranged in a stack together with interconnection and cooling means resulting in a 3-dimensional VLSI **integrated circuit**.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 12 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:253051 CAPLUS
DN 132:258213
TI **Interlayer dielectric** for **passivation** of an elevated **integrated circuit** image sensor structure
IN Theil, Jeremy A.; Ray, Gary W.; Perner, Frederick A.; Cao, Min
PA Hewlett-Packard Company, USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6051867	A	20000418	US 1999-306238	19990506
	JP 2001024059	A2	20010126	JP 2000-127497	20000427
	EP 1052698	A2	20001115	EP 2000-303822	20000508
	EP 1052698	A3	20010829		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
PRAI	US 1999-306238	A	19990506		

AB The **integrated circuit** sensor structure includes a substrate which includes electronic circuitry. An interconnect structure is adjacent to the substrate. The interconnect structure includes conductive interconnect vias which pass through the interconnect structure. A **dielec. layer** is adjacent to the interconnect structure. The **dielec. layer** includes a planar surface, and conductive dielec. vias which pass through the **dielec. layer** and are elec. **connected** to the interconnect vias. The **dielec. layer** further includes an **interlayer** planarization **dielec. layer** adjacent to the interconnect structure, and a **passivating layer** adjacent to the **interlayer** planarization **dielec. layer**. The **integrated circuit** sensor structure further includes sensors adjacent to the **dielec**

. **layer**. The interconnect vias and the dielec. vias elec. connect the electronic circuitry to the sensors.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 13 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:769620 CAPLUS
DN 133:316348
TI Anisotropic electroconductive adhesive and electrically conducted structure therewith
IN Kato, Shinichi
PA Casio Computer Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000306428	A2	20001102	JP 1999-111830	19990420
PRAI JP 1999-111830		19990420		

AB The adhesives, which are originally dielec., disperse electroconductive particles having corners or projections and bilayer **coatings** of **insulation** lower **films** and electroconductive upper films. The particles may be Ni and the electroconductive films may be Ni platings. The adhesives keeps good elec. interconnection between, for example, bump contacts in LCD substrates and terminals of semiconductor **chips**.

L11 ANSWER 14 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1999:671065 CAPLUS
DN 131:280155
TI Forming a moisture barrier guard ring structure for an **integrated circuit**
IN Liaw, Jhon-jhy
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5970346	A	19991019	US 1997-933370	19970919
US 6255715	B1	20010703	US 1999-378498	19990820
PRAI US 1997-933370	A3	19970919		

AB The invention provides a method for forming a moisture barrier guard ring structure around a fuse window in an **integrated circuit** . The invention begins by forming a fuse structure over the isolation regions and across the fuse window area. A cap **layer** and an interlevel **dielec. layer** (ILD) are formed over the fuse structure. A 1st ring (e.g., W contact plug) is formed over the isolation region surrounding the fuse window area and over the fuse structure. A key feature is that the 1st annular ring and the cap **layer** form a moistureproof **seal** over the fuse structure. A 1st conductive wiring line is formed over the 1st ring. Next, an intermetal **dielec.** (IMD) **layer** is formed over the ILD layer. A 2nd ring is formed through the IMD layer on the 1st conductive

wiring line. A 2nd conductive wiring line is formed over the 2nd ring. A **passivation layer** is formed over the resulting surface and a fuse window is etched through the **passivation layer** and partially through the IMD layer over the fuse window area. The 1st ring, the 1st conductive wiring line, the 2nd ring, and the 2nd conductive wiring line comprise the moistureproof guard ring structure surrounding the fuse window area.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 15 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1999:472156 CAPLUS
DN 131:137787
TI Electroconductive polymer **films** and **connection** of electronic components by flip **chip** mounting using thereof
IN Funada, Yoshitsugu; Ohuchi, Toshiyoshi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11203938	A2	19990730	JP 1998-1861	19980107
	JP 3422243	B2	20030630		
PRAI	JP 1998-1861		19980107		

AB The title polymer **films** comprise elec. **insulative** particles and elec. conductive particles contg. in an insulative polymer, wherein the elec. conductive particles are prepd. by **coating** of conductive metal **layer** around **insulative** particles. Both the insulative particles and the particle core for the conductive particles are made from elec. insulative inorg. particles such as **silica** particles. The conductive polymer films are easy for thermosetting in a short period of time and provides reliable connection in flip **chip** mounting.

L11 ANSWER 16 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1998:81114 CAPLUS
DN 128:135418
TI Fabrication of semiconductor memory devices having contact holes prepared by self alignment
IN Koga, Hiroki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10032314	A2	19980203	JP 1996-184425	19960715
	JP 2891192	B2	19990517		
PRAI	JP 1996-184425		19960715		

AB The title fabrication involves forming gate electrodes over a gate oxide film on a p-Si substrate, coating on the sides and the top of the gate electrodes with a 1st **silica** thin **film**, **coating** the entire surface over the electrodes with a Si3N4 thin

film, depositing over the entire surface with a thick BPSG film, chem.-mech. polishing the BPSG film selectively over the gate electrodes to expose the Si3N4 film through a contact hole in the BPSG film, and subsequently dry etching the exposed Si3N4 film through the contact hole over a resist mask to expose a lower contact on the substrate. The arrangement provides a precision contact hole for **connecting** a conductive contact **layer** on the highly **integrated** substrate without short-**circuiting** the gate electrodes.

L11 ANSWER 17 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1998:716155 CAPLUS
DN 129:324876
TI **Integrated circuit** having multilevel interconnections
IN Asano, Shintaro
PA Nec Corporation, Japan
SO Eur. Pat. Appl., 18 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 874398	A2	19981028	EP 1998-107252	19980421
	EP 874398	A3	19991013		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 10294363	A2	19981104	JP 1997-103096	19970421
	JP 3098450	B2	20001016		
	TW 393696	B	20000611	TW 1998-87106208	19980420
	CN 1199241	A	19981118	CN 1998-109259	19980421
	CN 1113394	B	20030702		
	US 5892284	A	19990406	US 1998-63712	19980421
PRAI	JP 1997-103096	A	19970421		

AB An **integrated circuit** includes upper and lower substrate interconnection layers which are positioned in a scribing line area and which are sepd. from each other by an **interlayer insulating film**. For planarization, the upper surface of the **interlayer insulating film** is **coated** with a SOG Si oxide **insulating film** formed from an org. soln. by spin coating. The lower substrate interconnection layer is divided into a plurality of segments sepd. from each other by gaps which are provided at a plurality of different locations and which allow the SOG org. soln. to escape through the gaps by centrifugal force when the SOG org. soln. is applied by spin coating. The upper substrate interconnection **layer** is elec. **connected** to the plurality of segments of the lower substrate interconnection layer through contact holes formed through the **interlayer insulating film**.

L11 ANSWER 18 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1996:307523 CAPLUS
DN 124:357978
TI Manufacture of insulated-gate TFT and **integrated circuit**
IN Yamazaki, Shunpei; Takemura, Yasuhiko
PA Handotai Energy Kenkyusho, Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08023100	A2	19960123	JP 1994-180950	19940707
	JP 3253808	B2	20020204		
	JP 2001203367	A2	20010727	JP 2000-365654	19940707
	JP 2002033487	A2	20020131	JP 2001-143620	19940707
	JP 2002033488	A2	20020131	JP 2001-143656	19940707
	JP 2002050768	A2	20020215	JP 2001-143550	19940707
	JP 2002057345	A2	20020222	JP 2001-143559	19940707
	US 5644147	A	19970701	US 1995-498532	19950705
	US 5818070	A	19981006	US 1997-811299	19970304
PRAI	JP 1994-180950	A3	19940707		
	US 1995-498532	A3	19950705		

AB The TFT has a bottom gate electrode, a top gate electrode with an anode oxide coating, and a pair of silicide regions on the outer sides of a pair of source/drain regions. The **integrated circuit** has a first interconnection in the same layer with the TFT bottom electrode and a second interconnection with an anode oxide **coating** in the same **layer** with the TFT top layer, having the same potential, and a third interconnection in the same layer with the TFT source/drain interconnection. The third interconnection does not cross the second interconnection and crosses the first interconnection via a first insulator. The manuf. of the **integrated circuit** involves forming a first gate interconnection, a first **insulator**, an island semiconductor **layer**, a second **insulator**, and a second gate interconnection in the order, anodic oxidn. of the second gate interconnection, doping in the semiconductor layer with the second gate interconnection and the anodic oxide coating as masks (self align), and forming a third interconnection **connected** to the semiconductor **layer**.

L11 ANSWER 19 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1995:772997 CAPLUS
DN 123:185626
TI Passivation method and structure for a ferroelectric **integrated circuit** using hard ceramic materials or the like
IN Argos, George, Jr.; Spano, John D.; Traynor, Steven D.
PA Ramtron International Corp., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5438023	A	19950801	US 1994-212495	19940311
	US 5578867	A	19961126	US 1995-394467	19950227
	JP 08055850	A2	19960227	JP 1995-52145	19950313
	JP 2921556	B2	19990719		
PRAI	US 1994-212495		19940311		

AB A method for passivating an **integrated circuit** includes the RF sputtering of a hard **passivation layer** on the surface of the **integrated circuit**. The hard **passivation layer** can be a ceramic material such as various doped and undoped titanates, zirconates, niobates, tantalates, stannates, hafnates, and manganates, in either their ferroelec. or

nonferroelec. phases. Other exotic, hard, and usually nonferroelec. materials not normally found in **integrated circuit** processing, such as carbides, may also be used. If the **integrated circuit** sought to be passivated contains ferroelec. devices, the hard **passivation layer** can be fabricated out of the same material used in the integrated ferroelec. devices. An optional SiO2 **insulating layer** can be deposited on the surface of the **integrated circuit** before the hard **passivation layer** is deposited. The optional SiO2 layer is used to prevent any possible contamination of the **integrated circuit** by the **passivation layer**. Similarly, an optional **sealing layer** such as SiO2, Si nitride, or polymer-based materials can be deposited on top of the **passivation layer** to prevent any possible contamination of the **integrated circuit** package by the **passivation layer**. Once the hard **passivation layer** and any optional layers are formed, these layers are etched to provide access to underlying **integrated circuit** bonding pads.

L11 ANSWER 20 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1995:705277 CAPLUS
DN 123:130075
TI Adhesives for multi-wired **integrated circuit** boards and manufacture of the circuit boards
IN Ariga, Shigeharu; Shinada, Eiitsu; Okamura, Toshiro; Iwasaki, Yorio; Murakami, Kanji; Nakazato, Juichi
PA Hitachi Chemical Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07022751	A2	19950124	JP 1993-164525	19930702
	JP 3324007	B2	20020917		
	US 5403869	A	19950404	US 1993-107115	19930817
	US 5486655	A	19960123	US 1994-345457	19941121
PRAI	JP 1992-217814	A	19920817		
	JP 1993-164525	A	19930702		
	US 1993-107115	A3	19930817		

AB The adhesives comprise epoxy compds., a cationic photochem. polymn. initiator, and a Sn compd. adsorbed on an inorg. filler. The manufg. involves **coating** an **adhesive layer** on an **insulated** substrate, wiring on the **adhesive layer** with **insulated** wires, partially curing the **adhesive layer** by photo-irradn., hot pressing the substrate, and subsequently addnl. photo-irradiating to complete the hardening of the **adhesive layer** so as to setting the wires firmly on the substrate. The adhesive and the manufg. process gives the circuits a precision and high-d. wiring without void formation.

L11 ANSWER 21 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1994:471700 CAPLUS
DN 121:71700
TI Resin-sealed semiconductor devices
IN Furuichi, Mitsuhiro
PA Nippon Electric Co, Japan

SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06069211	A2	19940311	JP 1992-245900	19920822
PRAI	JP 1992-245900		19920822		

AB The devices, comprising conductive films for under **layer** wirings successively **coated** with **interlayer insulating films** and conductive **films** for upper layer wirings in periphery of semiconductor **chips** sealed with resins, contain plural dummy conductive films, which are under the upper layer wirings and do not contact to the under layer wirings.

L11 ANSWER 22 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1991:596037 CAPLUS
DN 115:196037
TI Semiconductor **integrated circuit**
IN Akasaki, Hiroshi; Otsuka, Kanji
PA Hitachi, Ltd., Japan; Hitachi Cho LSI Engineering K. K.
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03057222	A2	19910312	JP 1989-191493	19890726
PRAI	JP 1989-191493		19890726		

AB In a semiconductor **integrated circuit** comprising a bump electrode on an electrode, which has been formed in an opening of a **coating film** on a semiconductor substrate, via a multilayer metal subbing **layer**, the **adhesive layer** (1st metal **layer** of the subbing layer) consists of a metal and an additive element whose affinity toward the elements of the **coating film** is higher than that for the metal for improving the adhesive strength. A 2nd **layer** (a 2nd **adhesive layer**) of the subbing layer consisting of the same metal used in the 1st layer may be formed. The **coating film** may be a Si oxide **insulating film**, and the additive may be .gtoreq.1 element (s) selected from Si, Ti, and Al.

L11 ANSWER 23 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1990:110098 CAPLUS
DN 112:110098
TI Silicon semiconductor **integrated circuit** with final **passivation film**
IN Kagami, Teruyuki; Murakami, Susumu; Sugawara, Yoshitaka
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI JP 01158738 A2 19890621 JP 1987-316243 19871216
PRAI JP 1987-316243 19871216
AB A reliable Si semiconductor **integrated circuit**, suitable for plastic **sealing**, comprises an **insulator film** on a **passivation film** and contacts of a Si substrate, a Si nitride **film** on the **insulator film**, and an outermost **layer** for covering the **insulator** and Si nitride **films**.

L11 ANSWER 24 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1988:141705 CAPLUS
DN 108:141705
TI Use of dielectric barrier material in **integrated-circuit** fabrication
IN Erie, David G.; Roberts, Jon A.; Lee, Eddie C.
PA Honeywell Inc., USA
SO U.S., 6 pp. Cont. of U.S. Ser. No. 603,861, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 4717449	A	19880105	US 1986-890874	19860725

PRAI US 1984-603861 19840425
AB A 1st layer of metalization interconnects is formed on an **integrated-circuit** substrate, followed by a **dielec**. barrier **layer** (esp. TixOy) and a dielec. passivating material (esp. SiO2). A via hole wider than the 1st interconnect is plasma etched in the passivating material using a 1st etch gas, and a 2nd etch gas is used to remove the dielec. barrier material in the area of the via. A 2nd metalization interconnect **layer** is then formed, **connected** to the 1st interconnect layer in the via.

L11 ANSWER 25 OF 25 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1956:66337 CAPLUS
DN 50:66337
OREF 50:12365a-i,12366a-i,12367a-i,12368a-b
TI American Society for Testing Materials, Standards, 1955, VII. Textiles, soap, water, paper, adhesives, shipping containers, atmospheric analysis
SO (1955), 1658 pp.
DT Book
LA Unavailable
AB cf. C.A. 47, 8940a. Standards or tentative standards, adopted or revised in 1955 are given for: CaO and Ca(OH)2 for cooking rags in paper manuf.; CaO for sulfite pulp manuf.; waterproof paper for curing concrete; test for woven fabrics; textile testing machines; tire fabrics other than cord fabrics and tests therefor; definitions of terms relating to textile materials, soaps and other detergents, adhesives, shipping containers, industrial water and industrial waste water, atm. sampling and analysis, methods of mech. testing, sp. gr., and rheological properties of matter; tests and tolerances for cotton tire cord and cotton yarns; certain heavy cotton fabrics for manuf. of hose and belting and tests therefor; sampling and testing untreated paper used for elec. insulation; tests and tolerances for cotton sewing threads; numbered cotton duck and army duck; tests and tolerances for knit goods, woven tapes, and for certain light and medium wt. cotton fabrics; methods of identification of fibers in textiles; asbestos yarns and asbestos tapes and tests therefor; cotton

goods for rubber and pyroxylin coating and tests therefor; woven cotton tapes for elec. purposes; detg. relative humidity; tests and tolerances for certain carded cotton gray goods and for tubular sleeving and braids; test for thickness of solid elec. insulation; asbestos roving for elec. purposes and tests therefor; Holland cloth and tests therefor; tests for Cu and Mn in textiles; test for dimensional changes in laundering of fabrics woven wholly or partially of man-made org. base fibers; test for pile floor covering; fineness of wool and of wool tops and methods of test therefor; test for resistance to yarn slippage in silk, rayon, and acetate woven fabrics; tests for colorfastness to com. laundering and to domestic washing of cotton and linen textiles, and for colorfastness of dyed or printed wool, silk, rayon, or acetate fabrics to laundering or domestic washing; test for shrinkage in laundering of woven cotton cloth; milled toilet soap; caustic and modified sodas; soda ash; sampling and chem. analysis of soaps and soap products; testing felt; testing and tolerances for certain wool and part wool fabrics; **chip** soap; ordinary bar soap; powd. soap; white floating toilet soap; chem. analysis of sulfonated and sulfated oils; sampling and chem. analysis of alk. detergents; sampling and analysis of Na5P3O10; test for particle size of soaps and other detergents; test for colorfastness to light of textiles; sampling industrial water; tests for Ca ion, Mg ion, dissolved O, phosphate, total Al, Al ion, and nitrate ion in industrial water; tests for chloride ion, OH ion, SO4 ion, Mn, and SiO2 in industrial water and industrial waste water; test for total CO2 and calcn. of CO3 and HCO3 ions in industrial water; test for fiber length of wool tops; tests for bulking thickness and machine direction of paper; powd. built soap; alk. soap powder; palm oil solid and **chip** soaps; Na2SiO3; Na3PO4; test for apparent fluidity of dispersions of cellulose fibers; testing rayon and acetate staple; testing and tolerances for single jute yarn; test for water-sol. acidity or alky. of paper; test for rosin in paper and paperboard; test for viscosity and total solids content of rubber cements; testing woven asbestos cloth; testing and tolerances for glass yarns, woven glass fabrics, woven glass tapes, and woven glass tubular sleeving and braids; test for resistance of textile fabrics and yarns to insect pests; test for water resistance of textiles; test for wool content of raw wool; sampling paper and paper products; tests for ash content and opacity of paper and paper products; tests for .alpha.-, .beta.-, and .gamma.-cellulose and casein in paper; test for paraffin content of waxed paper; test for starch in paper; olive oil **chip** and solid, and salt-water soaps; Na sesquisilicate; Na4P2O7; reporting results of analysis of industrial water and industrial waste water; fire-retardant properties of treated textile fabrics; test for evaluating compds. designed to increase resistance of fabrics and yarns to insect pests; testing asbestos tubular sleeving; quant. analysis of textiles; conditioning paperboard, fiberboard, and paperboard containers for testing; compression test for shipping containers; test for folding endurance of paper; test for moisture in paper, paperboard, and paperboard and fiberboard containers; tests for thickness and basis wt. of paper and paper products; woven asbestos cloth; testing and tolerances for fine staple cotton gray goods, all-cotton, and cotton and rayon fine fancy goods, rayon tire cord, and of jute rove and plied yarn for elec. and packing purposes; test for color-fastness of dyed acetate to atm. fumes; test for resistance of textile materials to microorganisms; conditioning paper and paper products for testing; qual. examn. of mineral filler and mineral coating of paper; quant. detn. of **coating** on mineral-**coated** paper; test for pentosans in paper; test for internal tearing resistance of paper; compd. **chip** and powd. soaps; turpentine test for grease resistance of paper; test for degree of staining of paper by alkali; tests for surface wettability, and

of wire and felt sides of paper; test for resistance of paper to passage of air; test for kerosine number of roofing and flooring felt; test for air permeability of textile fabrics; testing and tolerances for rope made from bast and leaf fibers; testing and tolerances for spun, twisted, or braided products made from flax, hemp, ramie, or mixts. thereof; test for adhesiveness of gummed tape; test for bursting strength of paper; drop tests for shipping and cylindrical shipping containers; test for effect of heating on folding endurance of paper; test for flammability of treated paper and paperboard; test for pH of buffered paper exts.; test for water resistance of paper, paperboard, and other sheet materials; test for printing ink permeation of paper; test for puncture and stiffness of paperboard, corrugated and solid fiberboard; test for shipping containers; liquid toilet soap; chem. analysis of industrial metal cleaning compns.; corrosivity test of industrial water; testing rubber cements; chem. analysis of soaps contg. synthetic detergents; test for absorption by bibulous papers of water and writing ink; tests for ply adhesion, degree of wet curl, and for edge tearing strength of paper; tests for tensile breaking strength and for wet tensile breaking strength of paper and paper products; sampling water from boilers; designation of linear d. of fibers, yarns, and other textile materials in universal units; test for evaluating treated textiles for permanence of resistance to microorganisms; incline impact test for shipping containers; test for compatibility of glass yarn with insulating varnish; field sampling of water-formed deposits; tests for water vapor permeability of packages and of shipping containers; test for resistance of adhesive bonds to chem. reagents; test for tensile properties of adhesives; tests for applied wt. per unit area of dried adhesive solids and of liquid adhesive; test for peel or stripping strength of adhesives; detg. effect of artificial and natural light on permanence of adhesives; tests for strength properties of adhesives in shear, and in plywood type construction in shear; test for bleeding resistance of asphalted paper at elevated temp.; tests for blocking resistance and Cu no. of paper and paperboard; test for crease retention of wrapping paper; test for TiO2 in paper; NaHCO3; borax; total immersion corrosion test of water-sol. Al cleaners; tests for Fe and sulfate-reducing bacteria in industrial water and water-formed deposits; identification of cryst. compds. and the reporting results of examn. and analysis of water-formed deposits; corrosivity test of industrial water; mech. roll felt; test for impact strength of adhesives; test for water resistance of containers; drop test for bags; testing analytical filter papers; test for org. N in paper and paperboard; test for paraffin wax absorptiveness of paper; test for reducible S in paper; test for 45.degree., 0.degree. directional reflectance for blue light; prepn. of MgO standard for spectral reflectivity; test for stretch of paper and paper products under tension; test for water vapor permeability of paper and paperboard; recommended practice for interlab. testing of textile materials; test for penetration of liquids into submerged containers; vibration test for shipping containers; test for strength properties of adhesives in shear by tension loading; creasing paper for permeability test; test for ply sepn. of combined container board; test for peeling resistance of paperboard; test for fiber analysis of paper and paperboard; testing single kraft yarn; test for stretch of hosiery; test for yarn number of yarn from fabrics; core sampling of raw wool in packages for detn. of % of clean wool fiber present; asbestos lap and methods of test therefor; test for cleavage strength of metal-to-metal adhesives; sampling steam; tests for acidity and basicity, Fe, and suspended and dissolved matter in industrial water and industrial waste water; absorbent laminating paper for elec. insulation; testing large shipping cases and crates; test for consistency of adhesives; static bending test for

corrugated paperboard; test for water-sol. sulfates in paper and paperboard; filter paper for use in chem. analysis; **chip** or granular, and solid soaps for low-temp. washing; test for vegetable matter and alkali-insol. impurities in scoured wool; mech. sheet felt; test for snag resistance of hosiery; test for resistance of pile floor coverings to insect pest damage; testing bonded fabrics; test for magnetic rating of asbestos used for elec. purposes; test for elec. cond. of industrial water; tests for hardness, residual Cl, nitrite ion, bromide and iodide ions, Na, and K in industrial water; identification of types of microorganisms in industrial water; substitute ocean water; recommended practice for detg. strength development of adhesive bonds; test for blocking point of potentially **adhesive layers**; test for effect of moisture and temp. on adhesive bonds; test for chloride content of paper and paper products; test for water-sol. matter in paper; test for lint of paper towels; test for ring crush of paperboard; test for pH of aq. solns. of soaps and detergents; test for foaming properties of surface-active agents; test for effect of bacterial contamination on permanence of adhesive prepns. and adhesive bonds; test for abrasion resistance of textile fabrics; tests for CHCl3-extractable matter and for fluoride ion in industrial water and industrial waste water; test for resistance of adhesives for wood to cyclic lab. aging conditions; test for strength of adhesives on flexural loading; testing pallets; equipment for sampling industrial water and steam; reagent water; testing adhesives for brake linings and other friction materials; test for pinholes in glassine and other greaseproof papers; tests for contrast gloss of paper at 57.5.degree. and for specular gloss of paper at 75.degree.; test for Zn and Cd in paper; test for flat crush of corrugated paperboard; test for flammability of clothing textiles; tests for shrinkage in laundering of knit cotton and knit rayon fabrics; testing twine made from bast and leaf fibers; sampling and testing staple length of wool in the grease; tolerances for filament acetate, nylon, and rayon yarns; recommended practice for designation of yarn construction; examn. of water-formed deposits by chem. microscopy; tests for chem. O demand of, and for sulfides in industrial waste water; scheme for analysis of industrial water and industrial waste water; test for dimensional changes of paper with changes in moisture conditions; test for buffering action of metal cleaners; total immersion corrosion test for soak tank metal cleaners; test for rinsing properties of metal cleaners; test for ave. fiber diam. of wool tops; test for alkali soly. of wool; test for relaxation and felting shrinkage in laundering of stabilized knit wool fabrics; testing and tolerances for yarns contg. wool; test for effect of mold contamination on permanence of adhesive prepns. and adhesive bonds; tests for Cl requirement and pH of industrial water and industrial waste water; test for odor of industrial waste water; test for tensile strength of wool fiber bundles; test for recovery of textile fabrics from creasing; test for adhesives relative to their use as elec. **insulation**; elec. **insulating** paper, **interlayer** type; test for tensile strength of paraffin wax; test for needle penetration of petroleum waxes; test for surface and interfacial tension of solns. of surface-active agents; test for detn. of build-up and spread of glass yarn as wrap or braid over elec. conductors; testing elastic fabrics; test for tuft bind of pile floor coverings; test for yarn distortion in woven fabrics; test for storage life of adhesives; test for working life of liquid or paste adhesives; test for sulfite ion in industrial water; test for oily matter in industrial waste water; detn. of thickness of internal deposits on tubular heat exchange surfaces; testing cross-lap specimens for tensile properties of adhesives; test for evaluating acute toxicity of industrial waste water to fresh-water fishes; detg. concns. of odorous vapors;

continuous analysis and automatic recording of SO2 content of the atm.; planning the sampling of the atm. for analysis; testing package cushioning materials; aerated total immersion corrosion test for metal cleaners; test for pilling propensity of textile fabrics; testing of warp knit and of wide elastic fabrics; test for absorbency time and absorptive capacity of nonwoven fabrics; test for abrasion resistance of textile yarns; testing spun and filament yarns made wholly or in part of man-made org. base fibers; fineness of mohair tops and methods of test therefor; test for susceptibility of dry **adhesive films** to attack by roaches and lab. rats; test for hydrazine in industrial water; test for stiffness of fabrics; test for length and length distribution of cotton fibers; sampling cotton fibers for testing; test for fiber wt. per unit length and maturity, cross-sectional characteristics, strength, number of neps, length, and micronaire fineness of cotton fibers; detg. specific area and immaturity ratio of cotton fibers; methods of verification of testing machines; sieves for testing purposes; definition of term screen; designating significant places in specified limiting values; definitions with procedures relating to conditioning and weathering; operation of light- and water-exposure app. for artificial weathering test; detn. of pH of aq. solns. with glass electrode; verification of calibration devices for verifying testing machines; test for measuring water vapor transmission of materials in sheet form; test for 45.degree., 0.degree. directional reflectance of opaque specimens; probability sampling of materials; and detn. of Young's modulus at room temp. Tentative revisions submitted in 1955 are given for testing and tolerances for certain wool and part wool fabrics; testing pile floor covering; waterproof paper for curing concrete; and definitions of terms relating to adhesives.

L21 ANSWER 1 OF 3 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:319205 CAPLUS
DN 138:346238
TI Light emitting device and method of manufacturing a semiconductor device
IN Yamazaki, Shunpei; Kuwabara, Hideaki
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO U.S. Pat. Appl. Publ., 61 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003075733	A1	20030424	US 2002-238050	20020910
	JP 2003186421	A2	20030704	JP 2002-263583	20020910
PRAI	JP 2001-273912	A	20010910		
	JP 2001-282714	A	20010918		

AB A light emitting device is described comprising at least one pixel and at least one light emitting element in a pixel portion formed on an insulating surface, wherein the pixel portion comprises at least first and second thin film transistors, wherein the first thin **film** transistor is **connected** to a pixel electrode that is an anode or a cathode of the light emitting element, wherein the light emitting element comprises a layer comprising an org. compd. as a light emitting layer, and wherein the first and second thin film transistors have the same channel length direction, thereby reducing the dispersion of ON current of thin film transistors. Semiconductor layers for serving as active layers of a plurality of thin film transistors in a driving circuit and in a CPU may be arranged in the same direction, and may be irradiated with laser light with the scanning direction matched to the channel length direction of the semiconductor layers. A method of fabricating a semiconductor device is also described entailing forming a first electrode on a substrate that has an insulating surface; forming a first **insulating film** on the first electrode; leveling a surface of the first **insulating film**; forming a semiconductor **film** on the first **insulating film**; irradiating continuous wave laser light to crystallize the semiconductor **film**; forming a second **insulating film** on the semiconductor film; a seventh step of selectively etching the first **insulating film** and the second **insulating film** to form a contact hole that reaches the first electrode; and decreasing impurities on a surface of the second **insulating film**; forming a second electrode that is elec. connected to the first electrode through the contact hole and partially overlaps the semiconductor **film** on the second **insulating film**.

L21 ANSWER 2 OF 3 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:638051 CAPLUS
DN 137:176923
TI Light emitting device and method of manufacturing the same
IN Yamagata, Hirokazu; Yamazaki, Shunpei; Takayama, Toru
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO U.S. Pat. Appl. Publ., 44 pp.
CODEN: USXXCO
DT Patent
LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002113248	A1	20020822	US 2002-73284	20020213
	CN 1372325	A	20021002	CN 2002-104596	20020209
	JP 2002334790	A2	20021122	JP 2002-38053	20020215
PRAI	JP 2001-41195	A	20010219		

AB Light-emitting device comprising a thin-**film** transistor on an **insulator**; an **interlayer insulating film** on the thin **film** transistor; a first **insulating film** on the **interlayer insulating film**; an anode on the first **insulating film**; a wiring line for elec. **connecting** the thin **film** transistor to the anode; a bank over the first **insulating film**, edge portions of the anode, and wiring; a second **insulating film** on the anode and the bank; an org. compd. layer over the anode with the second **insulating film** interposed between them; and a cathode on the org. compd. layer are described in which the first **insulating film** comprise .gtoreq.1 of a diamond-like carbon film, a **silicon nitride** film, and/or a cured **film** formed by plasma **treatment** using .gtoreq.1 of hydrogen, nitrogen, halogenated carbon, hydrogen fluoride, and rare gas. Devices are also described which comprise a thin **film** transistor on an **insulator**; a first **interlayer insulating film** over the thin film transistor; an electrode over the first **interlayer insulating film**; a wiring line for elec. **connecting** the thin **film** transistor to the electrode, over the first **interlayer insulating film**; a second **interlayer insulating film** over the first **interlayer insulating film**, the electrode, and the wiring line; and an antistatic film over the second **interlayer insulating film**. Methods for fabricating the devices are also described.

L21 ANSWER 3 OF 3 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:241809 CAPLUS
DN 134:246236
TI Interconnect structure and method employing air gaps between metal lines and between metal layers
IN Zhao, Bin
PA Conexant Systems, Inc., USA
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6211561	B1	20010403	US 1998-193499	19981116
PRAI	US 1998-193499		19981116		

AB An interconnect structure and fabrication method are provided to form air gaps between interconnect lines and between interconnect layers. A conductive material is deposited and patterned to form a 1st level of interconnect lines. A first **dielec. layer** is deposited over the first level of interconnect lines. One or more air gaps are formed in the first **dielec. layer** to reduce **inter-layer** capacitance, intra-layer capacitance or both

inter-layer and intra-layer capacitance. At least 1 support pillar remains in the first **dielec. layer** to promote mech. strength and thermal cond. A **sealing layer** is deposited over the first **insulative layer** to **seal** the air gaps. Via holes are patterned and etched through the **sealing layer** and the first **dielec. layer**. A conductive material is deposited to fill the via holes and form conductive plugs therein. Thereafter, a conductive material is deposited and patterned to form a second level of interconnect lines.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT